模拟与数字电路

Analog and Digital Circuits

课程主页 扫一扫

第八讲： **竞争与时序逻辑 电路**

Lecture 8: **Hazards and Sequential logics**

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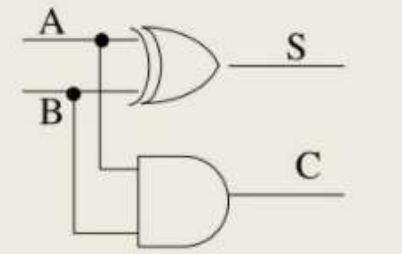
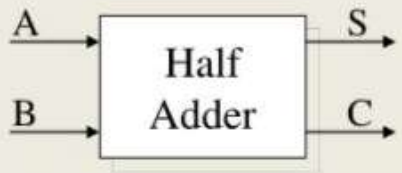
提纲

- 复习
  - 右图是一个半加器的Verilog
  - 试判断下图的模块的逻辑模块
- 竞争、冒险、毛刺
- 时序电路
- 锁存器



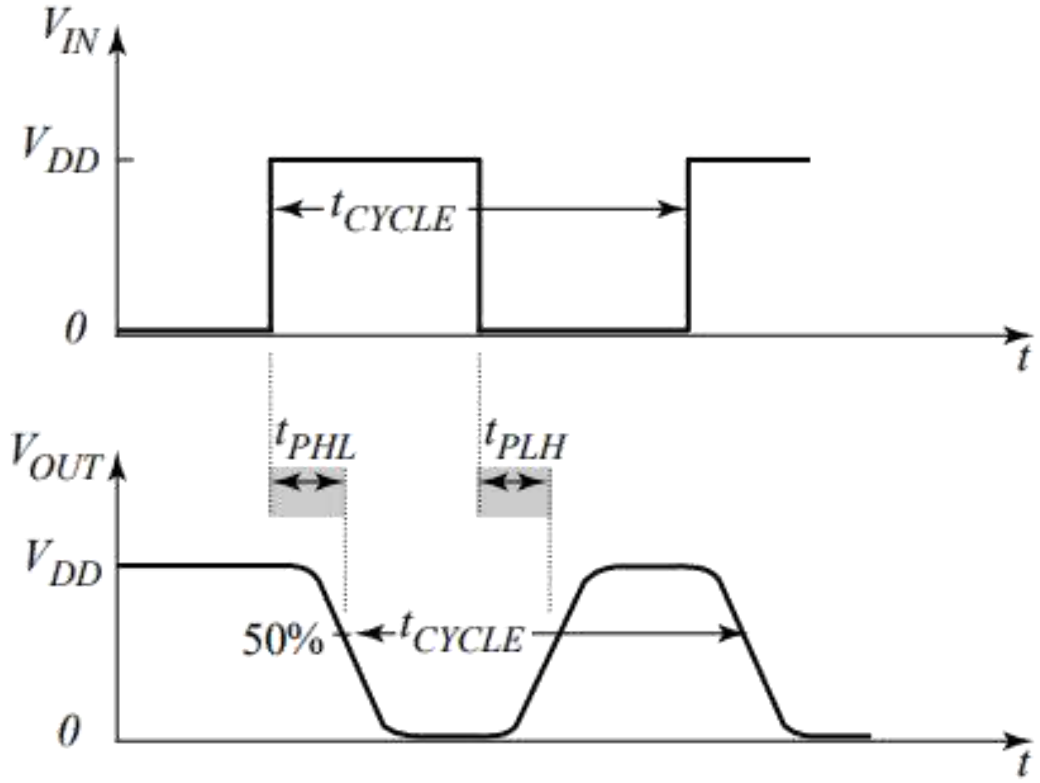


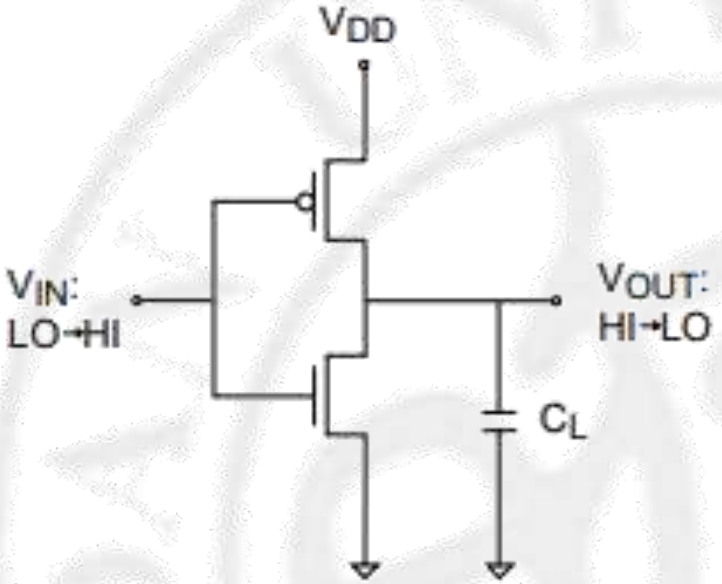

```
module half_adder(S, C, A, B);
output S, C;
input A, B;

wire S, C, A, B;

assign S = A ^ B;
assign C = A & B;

endmodule
```

```
module     XYZ     (S,C,x,y,z);
   input x,y,z;
   output S,C;
   wire S1,D1,D2; //Outputs of first XOR and two AND gates
//Instantiate the halfadder
    halfadder HA1 (S1,D1,x,y),
              HA2 (S,D2,S1,z);
    or g1(C,D2,D1);
endmodule
```

逻辑门延时

- 实际逻辑门存在延时

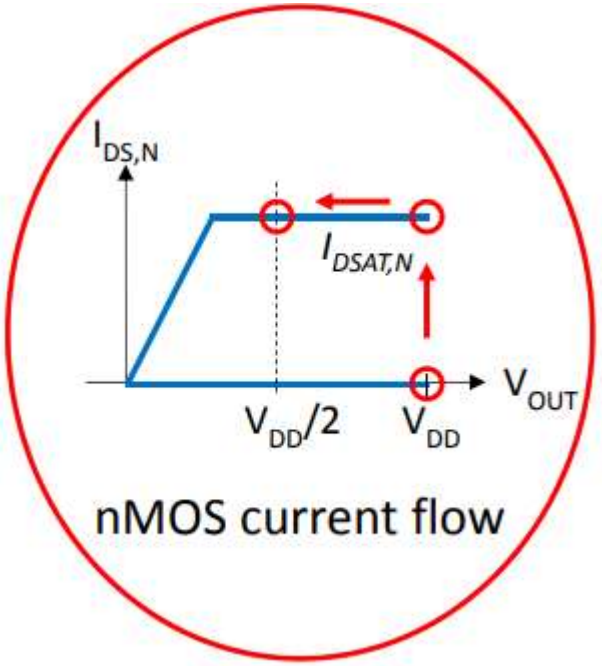


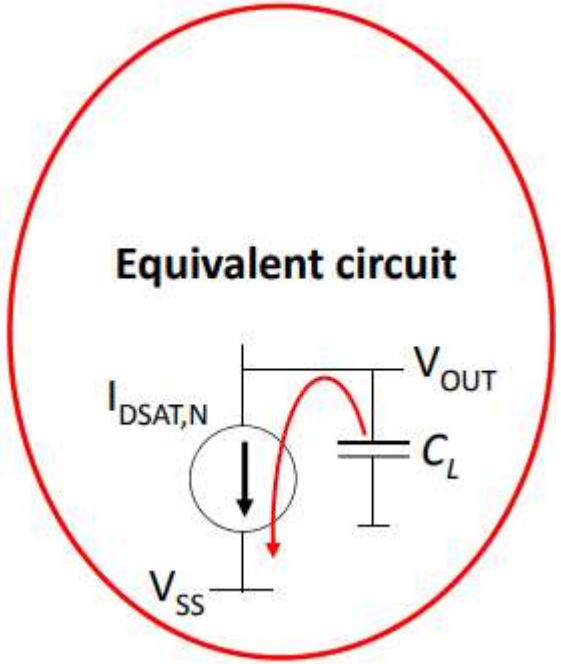


以反相器为例：延时是负载电容漏电、放电的过程

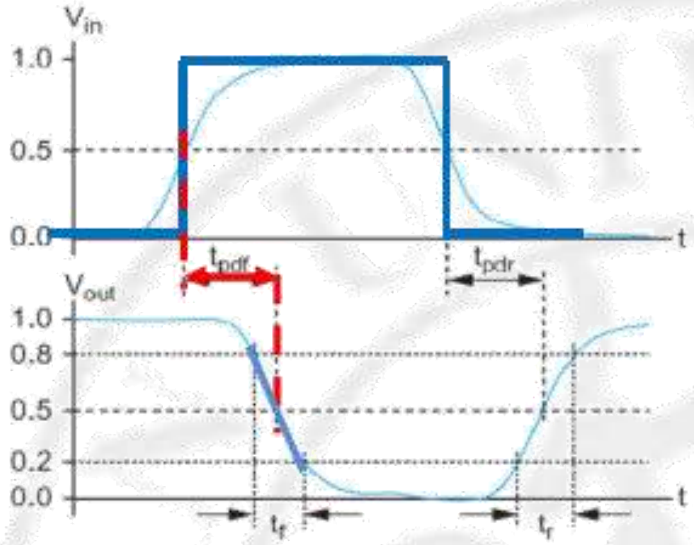
反相器延时

- 反相器输入 从低到高
  - 先进工艺下，反相器延时约在10ps





Square wave approximation

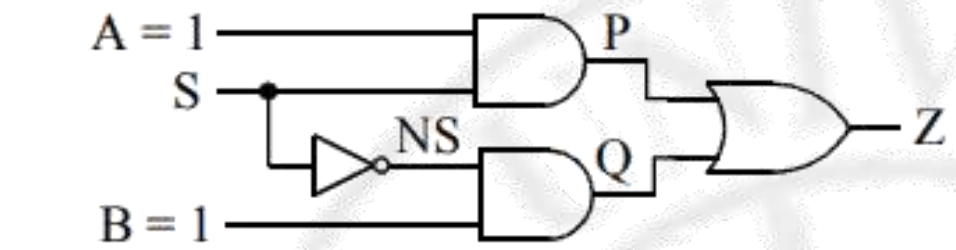


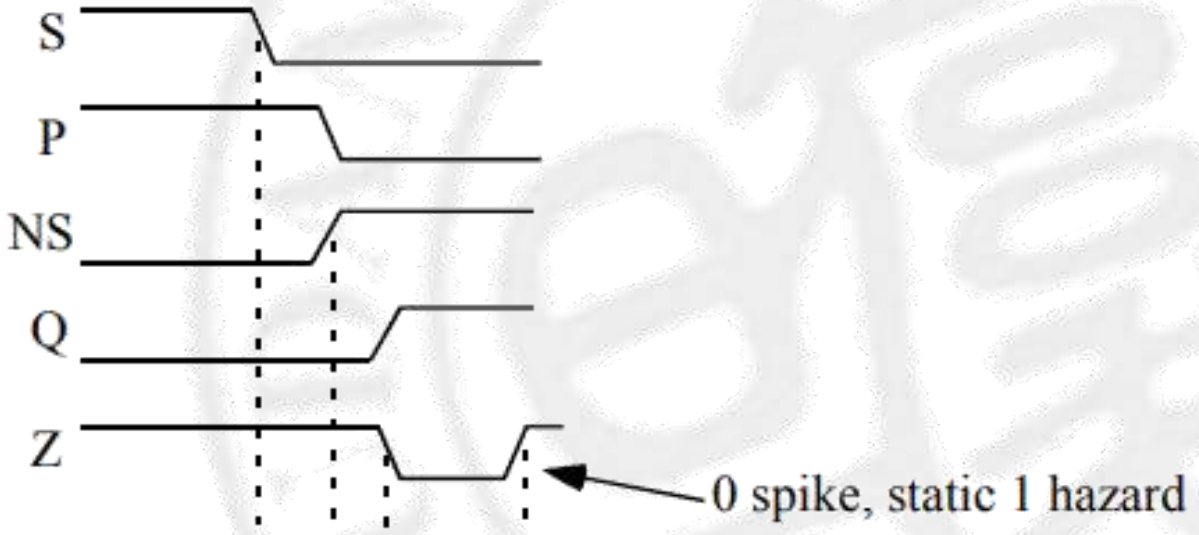
$$t_{pdr} = \frac{\Delta Q}{I_{DSAT,N}} = \frac{C_L \cdot \Delta V_{OUT}}{I_{DSAT,N}}$$

$\Delta V_{OUT}=V_{DD}/2$

Timing Hazards 竞争冒险

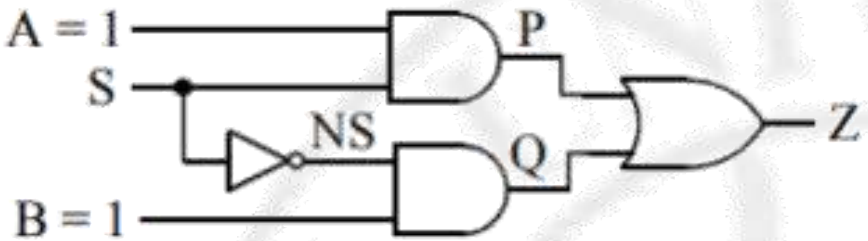
- 假设下列电路中的逻辑门具有相同的延时，在右图逻辑中：输入A/B保持不变，S从高到低，画出Z的时序波形。

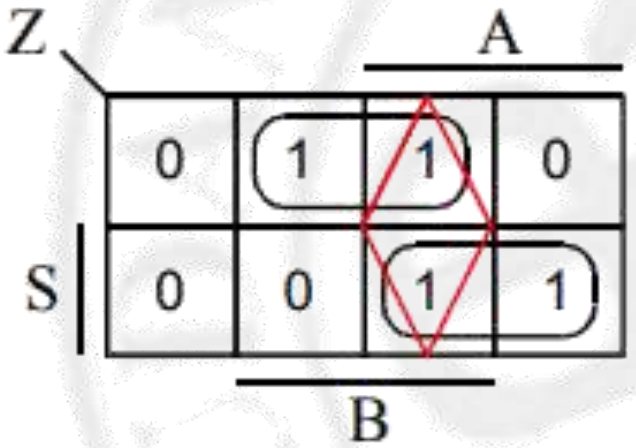




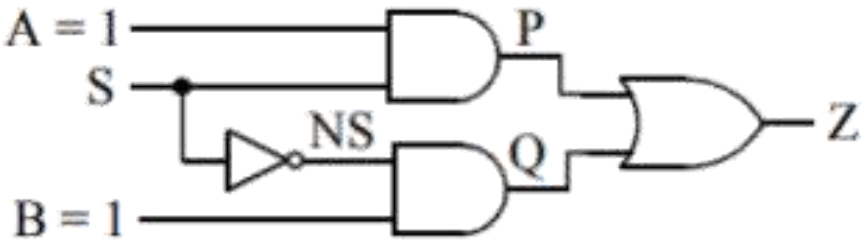
基于卡诺图的Hazard推断

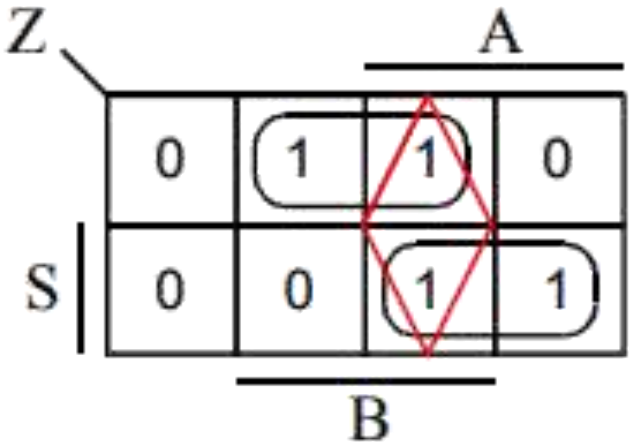
- Hazard原因：逻辑延时差
- 存在两个AND，其中一个AND门前没有非门，另一个前有非门
- 卡诺图上，相邻的格子均为1，但是，并未被同一个圈包裹

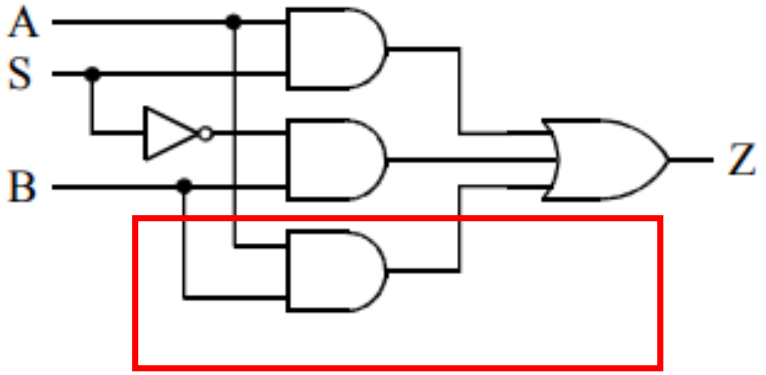




Hazard解决方案（一）：冗余项



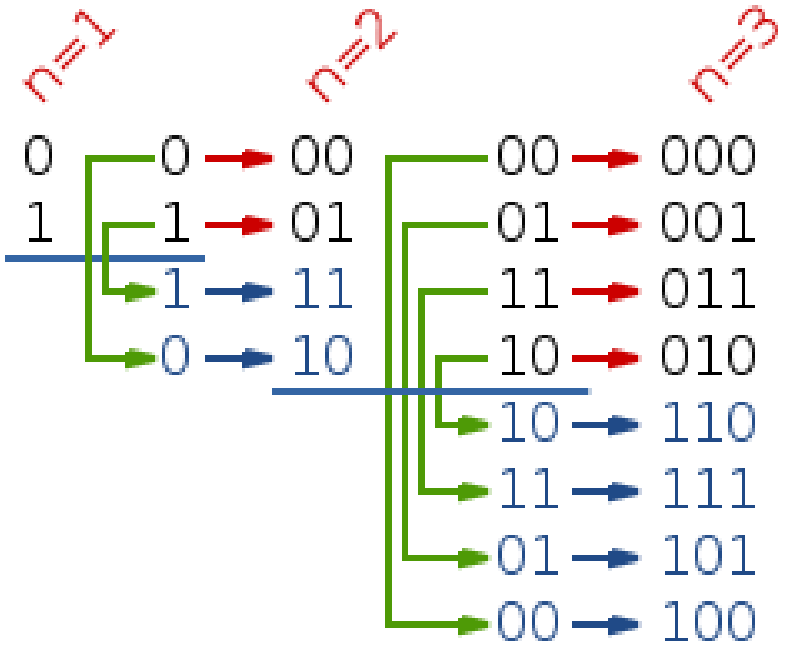




补充冗余项：将红色格子代表的门再次加回

Hazard解决方案（二）：专用编码

- 格雷码 Gray Code
  - 特点计数变化时，每次仅有1位变化



Decimal Number	4 bit Binary Number ABCD	4 bit Gray Code $G_1G_2G_3G_4$
0	0 0 0 0	0 0 0 0
1	0 0 0 1	0 0 0 1
2	0 0 1 0	0 0 1 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 1 1 0
5	0 1 0 1	0 1 1 1
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 0 0
8	1 0 0 0	1 1 0 0
9	1 0 0 1	1 1 0 1
10	1 0 1 0	1 1 1 1
11	1 0 1 1	1 1 1 0
12	1 1 0 0	1 0 1 0
13	1 1 0 1	1 0 1 1
14	1 1 1 0	1 0 0 1
15	1 1 1 1	1 0 0 0

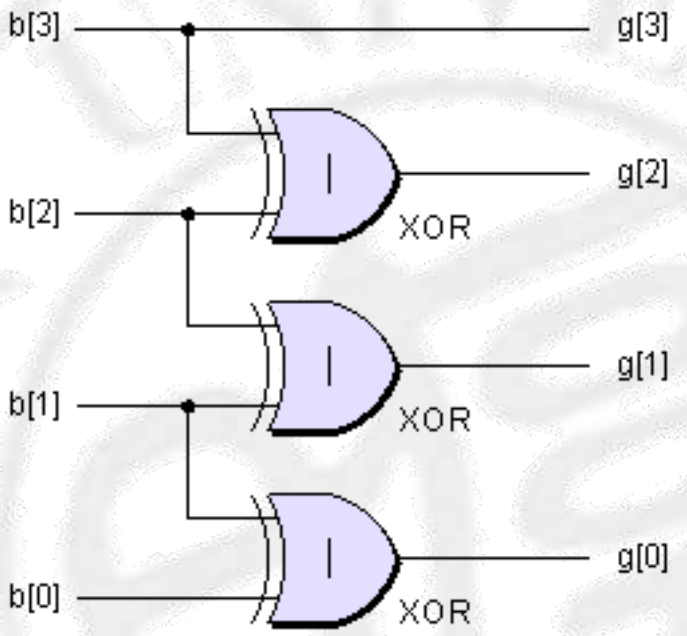
Hazard解决方案（二）：专用编码

- 格雷码的硬件实现（卡诺图）

b_3b_2 \ b_1b_0	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

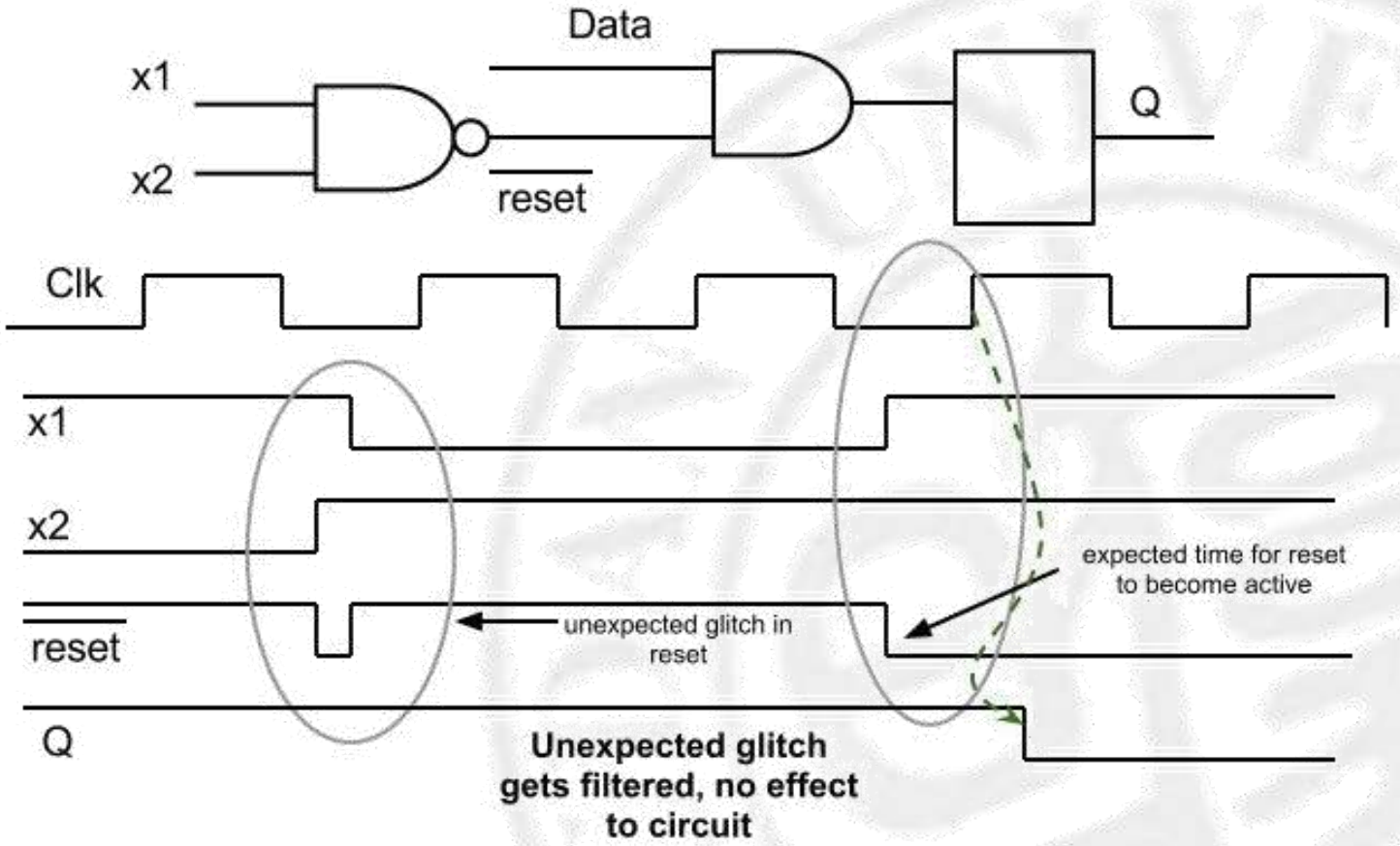
b_3b_2 \ b_1b_0	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	0	0	0	0
10	1	1	1	1

b_3b_2 \ b_1b_0	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	0
10	0	0	1	1



Hazard补偿方法（三）：同步时序电路

- 举例
  - 考试过程中的某个瞬间对错不在乎
  - 只关心交卷状态的成绩



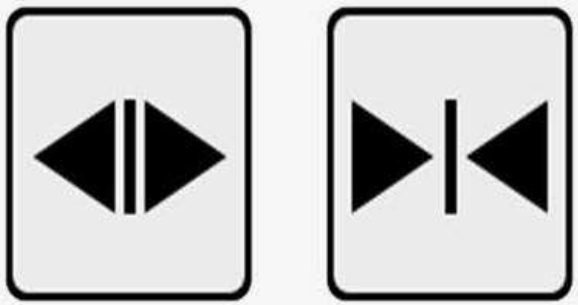
同步电路采用时钟才采样某个有效瞬间

时序逻辑 vs 组和逻辑

- 同步电路并不是组和逻辑，他存在一个器件使得

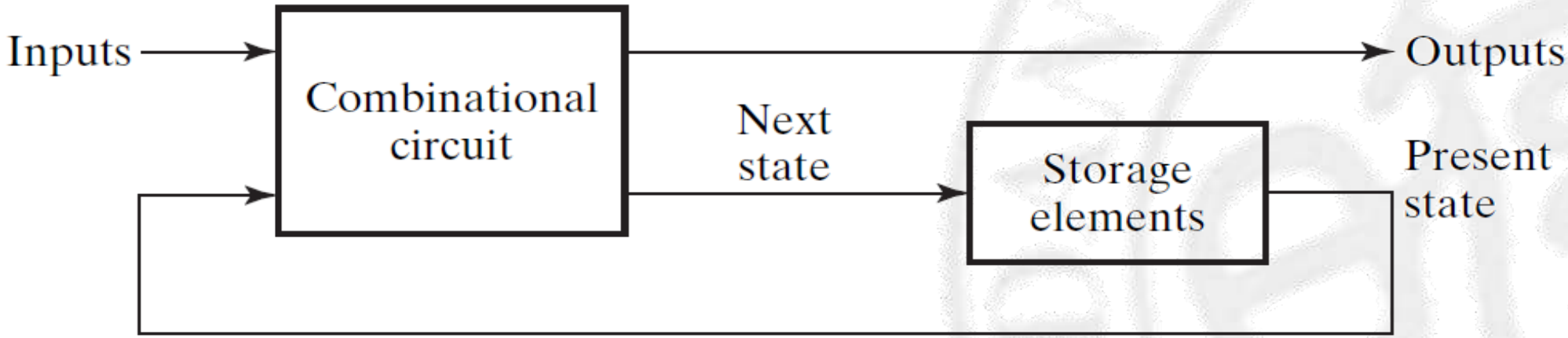
输出不仅跟当前的输入有关，而且**跟过去的输入也有关**。这就要求在电路中必须包含一些**存储元件**来记住这些输入的过去值。

- 生活中的时序逻辑
  举例：电梯开关门



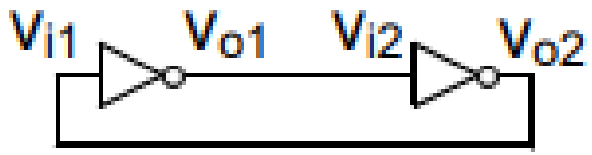
时序电路

- 组合逻辑+存储单元
- 输入和输出基于之前的状态与目前状态

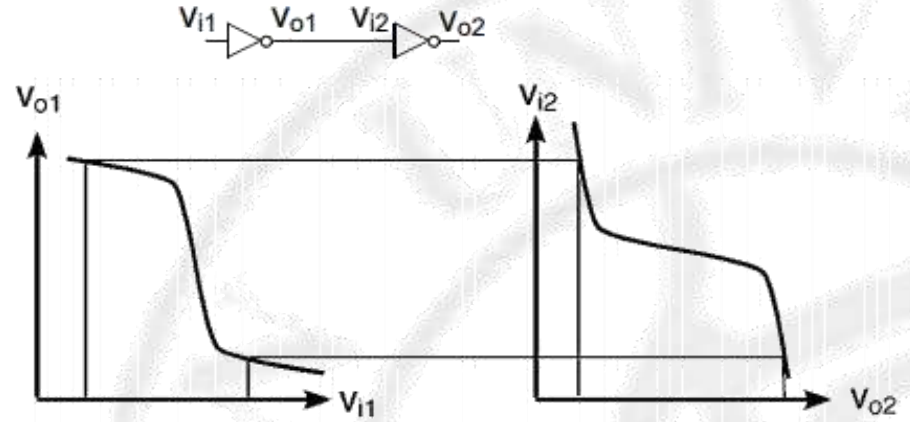


基于正反馈的存储单元

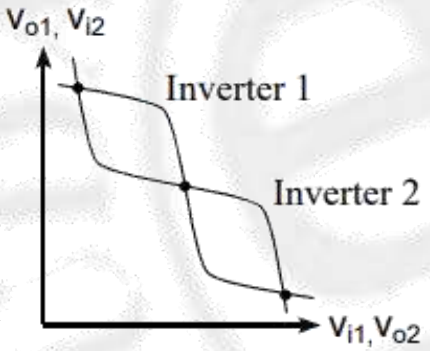
Latch可等效为反相器的级联
存在2-3个解
其中有一个是亚稳态



■ Now consider the behavior of the following circuit:



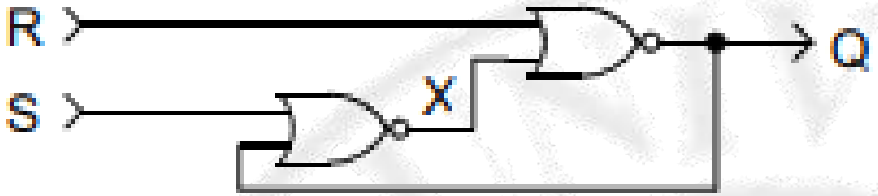
■ Superimposing the two graphs gives the following:

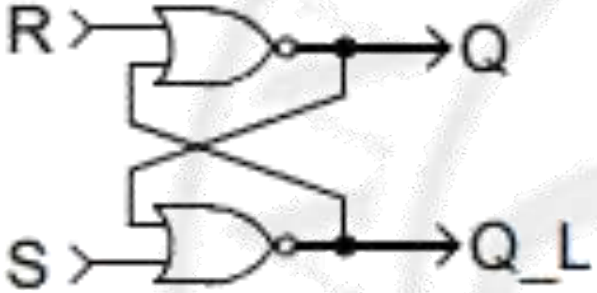


时序电路 基础原件： SR锁存器

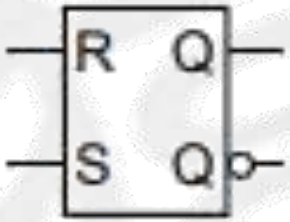
- 假设开关门逻辑存在两个输入: Set （关门）/ Reset （开门）
- 上述电路的真值表如下:

INPUTS		OUTPUT	STATE
S	R	Q	
0	0	No Change	Previous
0	1	0	Reset
1	0	1	Set
1	1	-	Forbidden





Logic Diagram

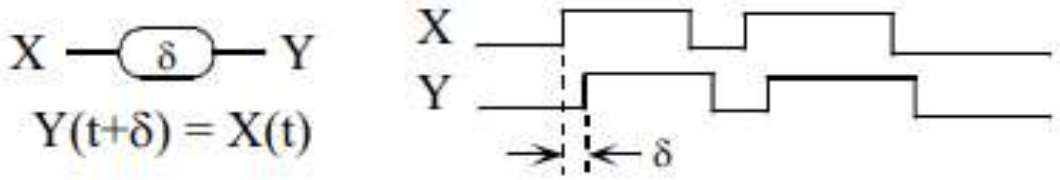


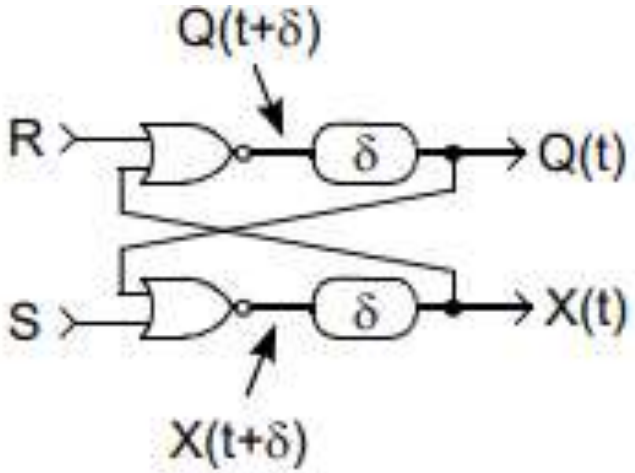
Symbol

SR 锁存器

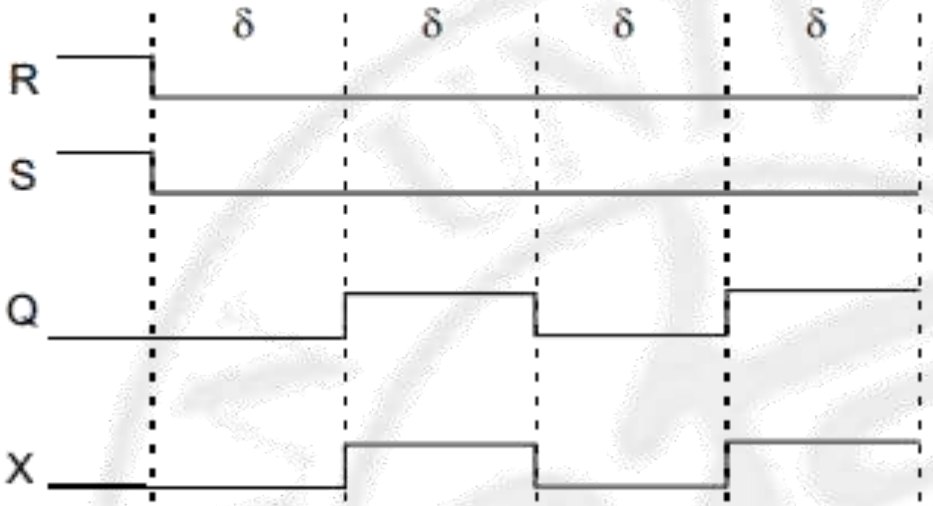
锁存器的非稳态实现

- 假设逻辑门存在延时 delta



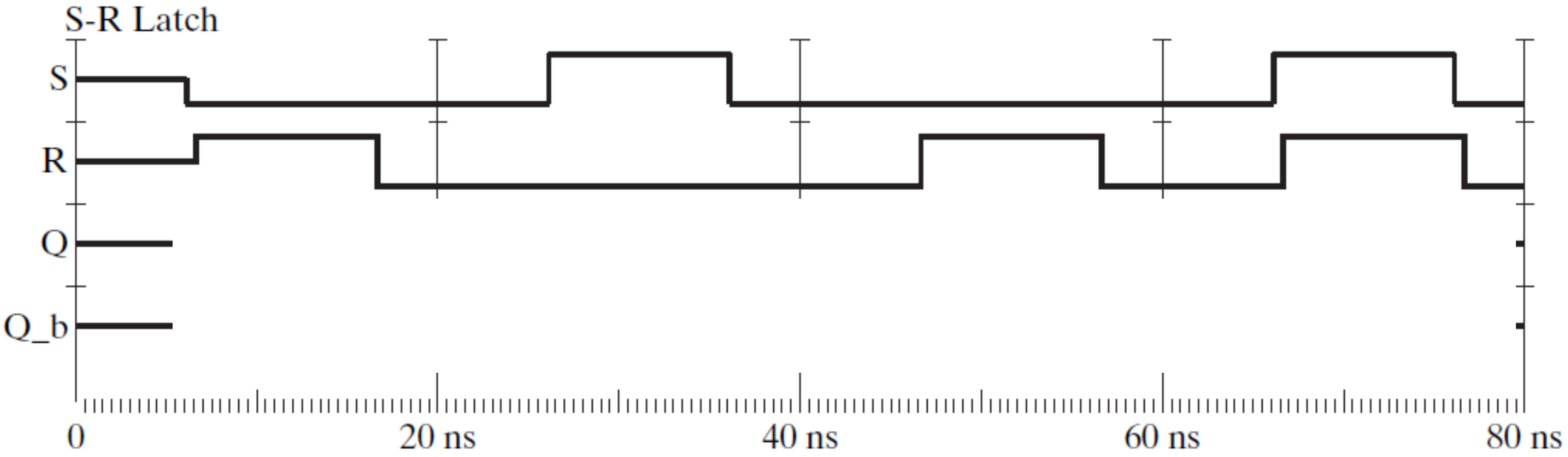


$Q(t+\delta) = X(t)'$ and $X(t+\delta) = Q(t)'$

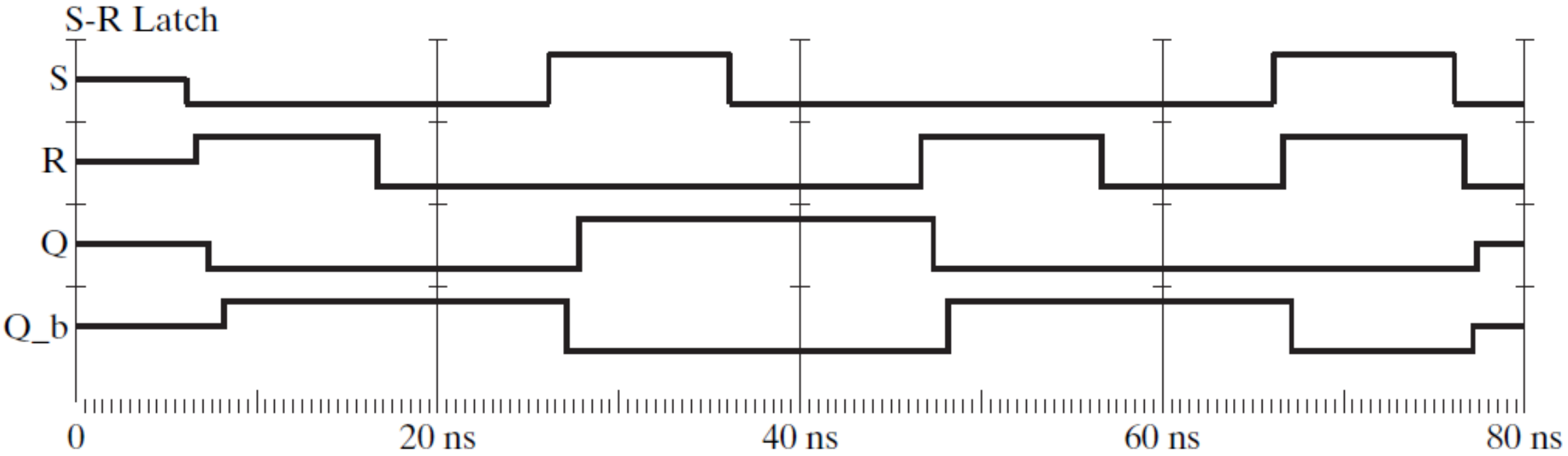


若SR存在同时由1到0的变化，存在延时delta1，那么锁存器电路可能振荡v

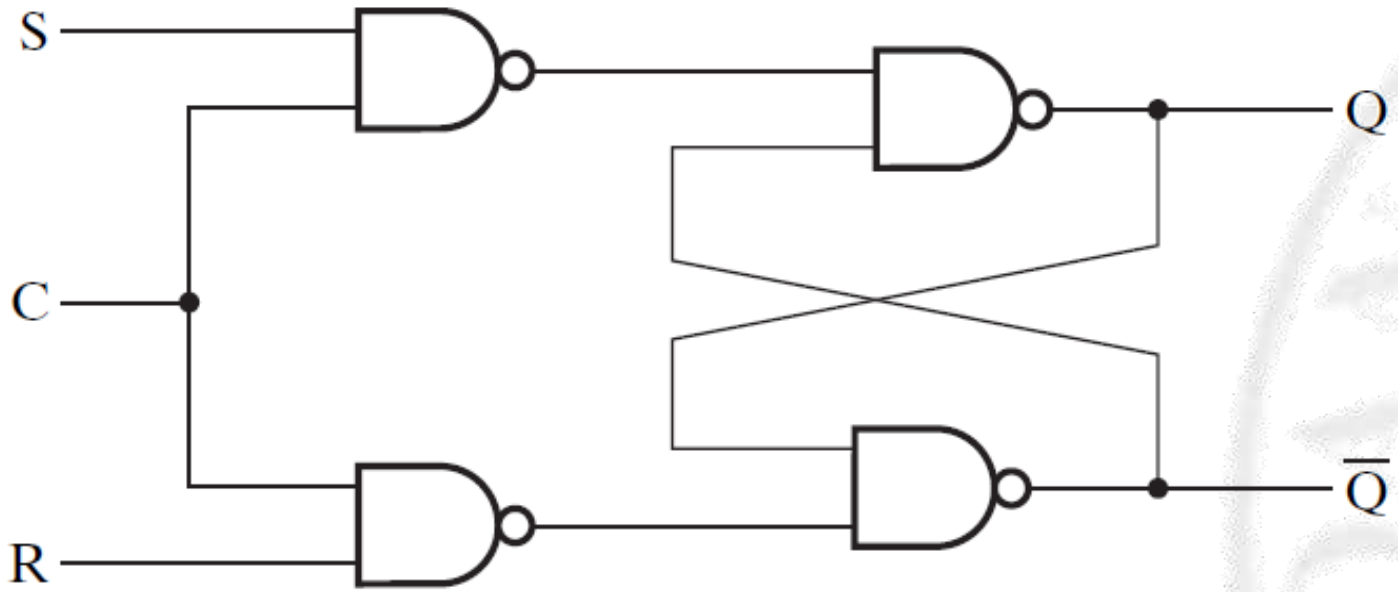
SR 锁存器波形



SR 锁存器波形



具有控制端的SR锁存器



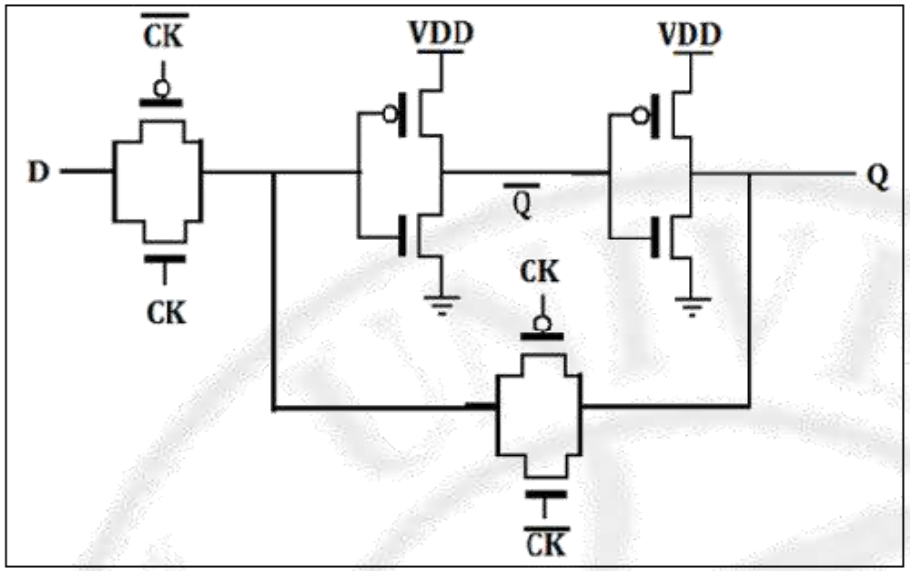
(a) Logic diagram

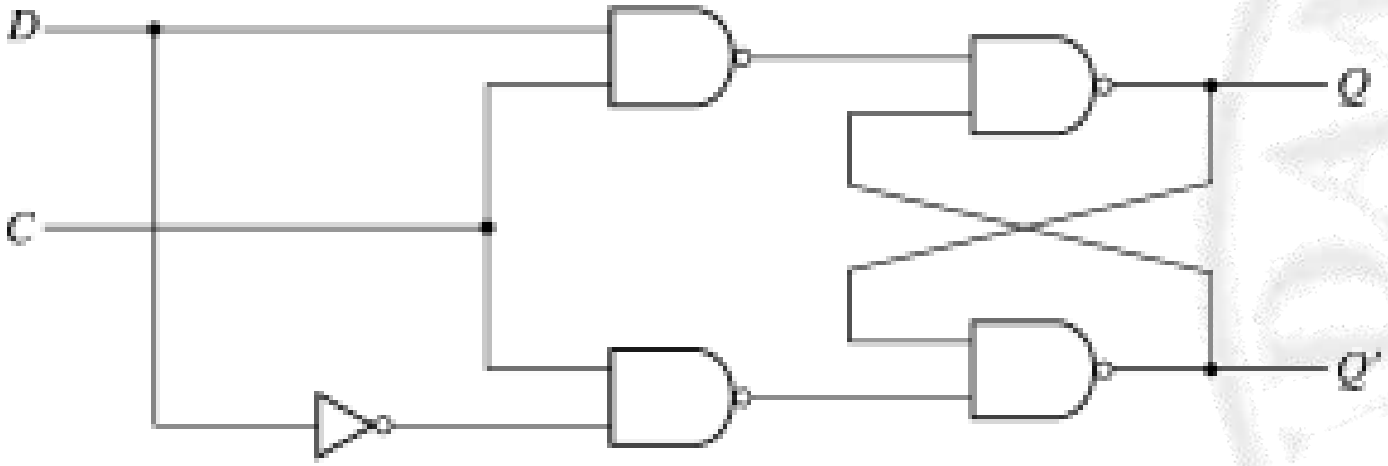
C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q = 0; Reset state
1	1	0	Q = 1; Set state
1	1	1	Undefined

(b) Function table

D型锁存器

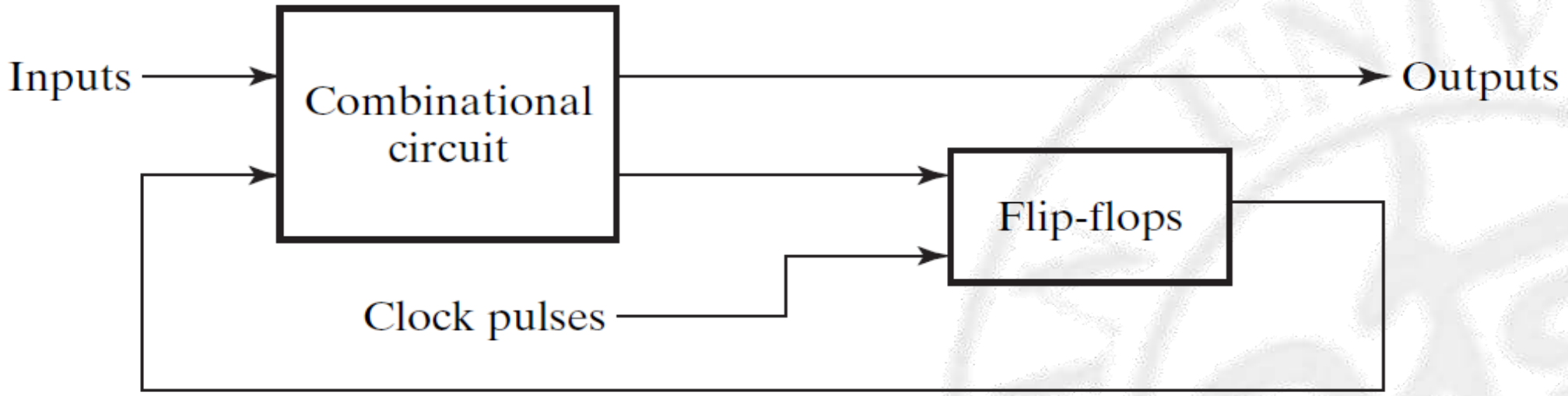
- D= Data
- 相比于输入端: 仅有数据输入，和使能（时钟输入）





C	D	Next state of Q
0	X	No change
1	0	$Q = 0$; Reset state
1	1	$Q = 1$; Set state

同步时序逻辑电路



(a) Block diagram

(b) Timing diagram of clock pulses