SME737006: Advanced Packaging & Integrated Chips **(Due: 05/2/25)**

Homework Assignment #2

Instructor: Chixiao Chen, Wenning Jiang *Name:* *, FudanID:*

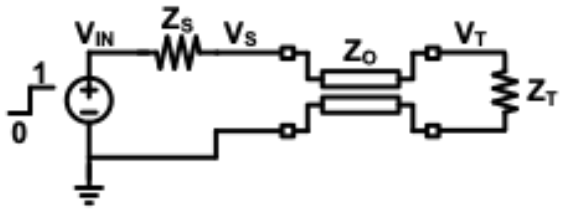
- This HW counts 15% of your final score, please treat it carefully.
- Please submit the electronic copy via mail: faet_english@126.com before 05/02/2025 11:59pm. Please use "Chiplet-Hmwk-2"+Your Name+Your FudanID as the mail title.
- It is encouraged to use LaTeX to edit it, the source code of the assignment is available via: https://www.overleaf.com/read/bqwfcnfpqsbg#8863f2
- You can answer the assignment either in Chinese or English

Problem 1: Signal Transmission and Reflection (40 points)

As shown in the figure, the source voltage is initially 0-V at time 0 ns. At 1 ns, the source generates a 1-V stepping signal. Assuming that:

- Source impedance: $Z_s = 100\,\Omega$
- Transmission line characteristic impedance: $Z_o = 50\,\Omega$
- Transmission line delay: $T_d = 1\,\text{ns}$
- Load impedance: $Z_t = 500\,\Omega$

Please 1) calculate the reflection coefficient at the load end, 2) calculate the voltage at the source end V_s and at the load end V_t for the first five time intervals, where each interval corresponds to one transmission delay T_d, with the detailed process 3) plot the voltage waveforms over time, illustrating voltage changes at both the source and load ends.



Problem 2: High-speed Link Paper Review (60 points)

Please write a summary report within two-pages (a4) about one of ISSCC high-speed link paper in recent 3 years, focus on the idea, improvement and comparison with the state-of-the-arts, excluding the one I have shown in the course.

A paper list pool is shown as follow, where rows in green are ISSCC 2024, in blue from ISSCC 2023, and in yellow from ISSCC 2022.

	时钟提升	TX均衡	RX均衡	速度/能效	调制方式
SK_Hynix_13.1	高SNR、低功耗时钟架构（快速唤醒）	----	----	35.4Gb/s/p	PAM3
南科大_13.5	抖动降低87%（CIJ）	XTC（5b-C-peaking）、可重构FS-FFE	----	64Gb/s/p 1.27pJ/b	PAM4
Samsung_13.6	WCK CDN优化（减少了60mA/die，16Gb/s）	Gain-controlled FFE(优化PVT性能)、ZQ校准优化RLM	CTLE与1-tap DFE合并使用，简化反馈路径	37Gb/s	PAM3
SK_Hynix_13.8	时钟校准（减小了四相偏移量65%）	----	Offset_calib(w 1-tap DFE）、用于检测的IO减小了DQ PAD的寄生电容39%	10.5Gb/s/p	----
Samsung_13.10	HCRG、DCC	Cap_EQ On chip EQ(周期更短)	Offset_calib（数字控制）	48Gb/s 0.67pJ/b	NRZ
Samsung_6.4	Phase-training(SYNC_G)	Cap_EQ(XTC)	DFE w double tail latch(减小了反馈时间)	32Gb/s	NRZ
Samsung_28.3	SWJC(调整温度码的转换)	FS-FFE 3bit C-peaking 松弛阻抗匹配	松弛阻抗匹配	16Gb/s	PAM4/NRZ
首尔大学_28.6	CEC(边沿校正器，修正4相相位误差、减小功耗)	Driver(PN over NP，更好的非线性) 2-tap Edge boosting（cap和T-coil）	----	32Gb/s 0.51pJ/b	NRZ
Samsung_28.2	WCK训练(调节电流、3ps)	ZQ编码（多路复用合并、优化了ISI和PSIJ、移除了2个T-coil）	----	27Gb/s	----
浦项科技大学_28.4	----	4-tap A-FFE(基于反相器、改善面积功耗摆幅)	----	20Gb/s 1.18pJ/b	NRZ
高丽大学_28.5	----	Di-code EQ(可提供合适CM电压)	INV-BASED TIA Di-code ECC（硬件开销更小） 无电容失配校准	10Gb/s 0.385pJ/b	Di-code
国立首尔大学_28.6	----	电容驱动链路(FFE)与Ground强制偏置技术组合		12Gb/s	NRZ
Samsung_28.7	无需高速DCC/CDR	----	----	20Gb/s 1.24pJ/b	DECS