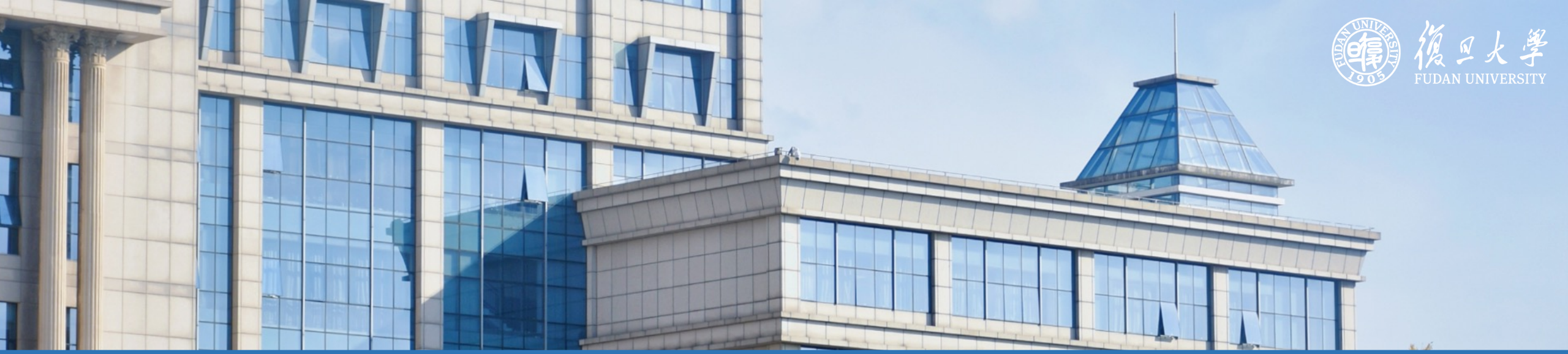


先进封装与集成芯片

Advanced Package and Integrated Chips

Lecture 4 : 3D & Bridge Technology

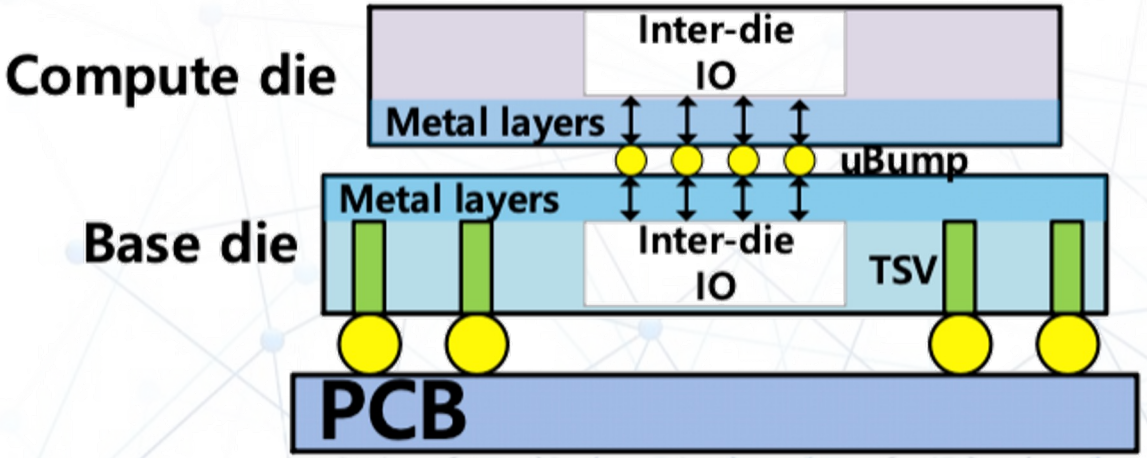
Instructor: Chixiao Chen, Ph. D

Overview

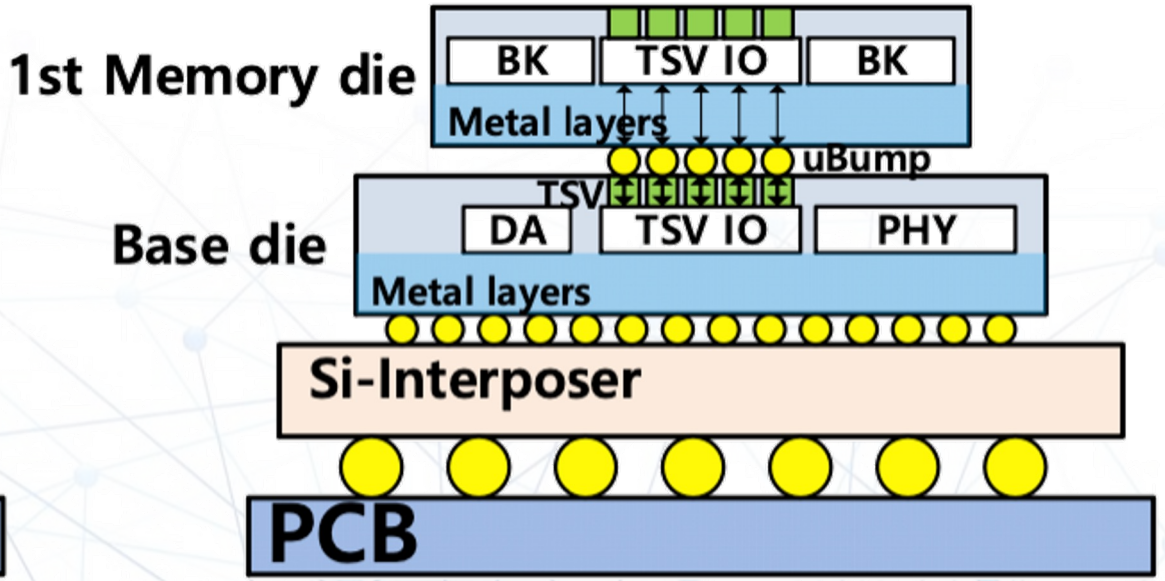
- 3D Integration Application (continued)
- Bridging Technology for 2.5D/3D Integration
- Design Consideration for 2.5D/3D Integration

3D Chip Stacking - I

- Typical 3D SoChiplet: BEOL + TSV(base die only) + micro-bumping (face to back)
- 3D Stacking Memory: TSV + micro-bump + BEOL (face to face)



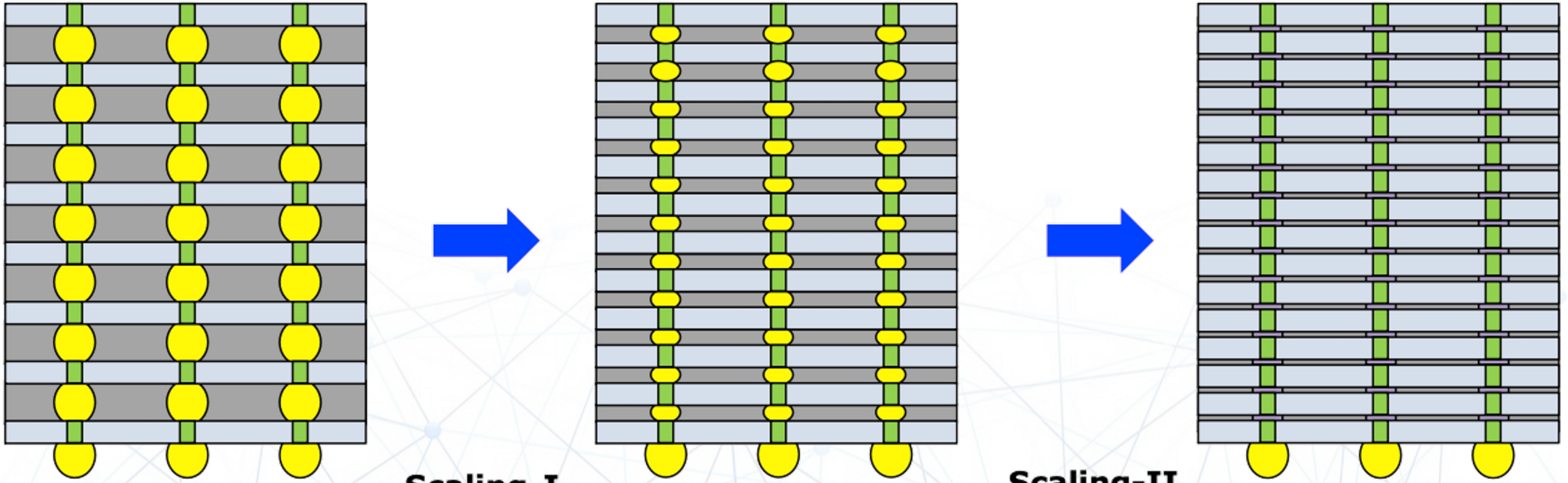
[W. Gomes, ISSCC 2020]
3D Mobile System



[K. Chun, ISSCC 2020]
High Bandwidth Memory (HBM2E)

3D Chip Stacking - II

- 8-stack → 12-stack (Dimensional Scaling) → 16-stack (New technology)



Scaling-I
uBump
Die thickness

[Source: AnandTech, "12-Layer 3D TSV DRAM"]

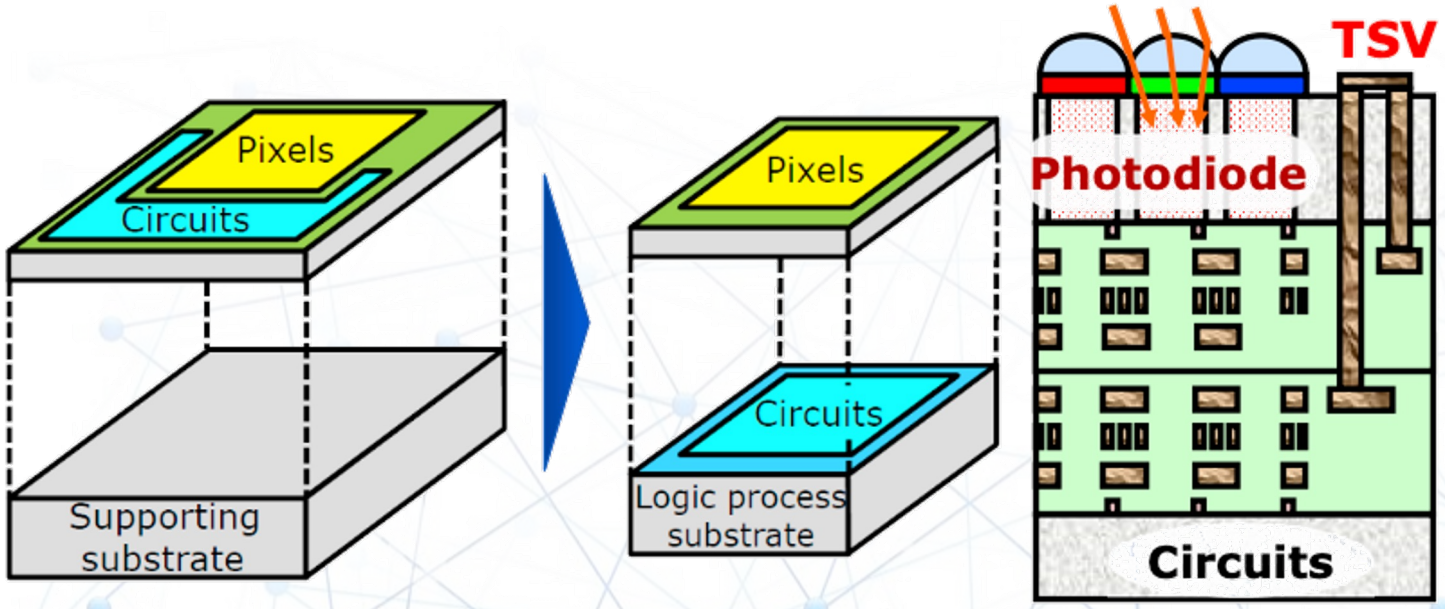
Scaling-II
uBump-less
D2W bonding

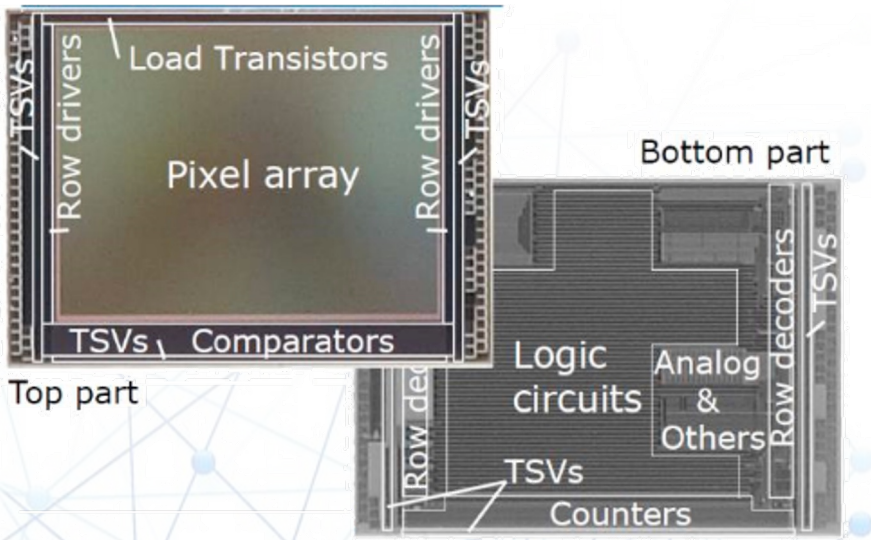
[Source: AnandTech, "DBI Ultra Interconnect"]

3D Stacked CMOS Image Sensor

- Stacked CIS has become mainstream in mobile cameras

Back-illuminated CIS Stacked CIS

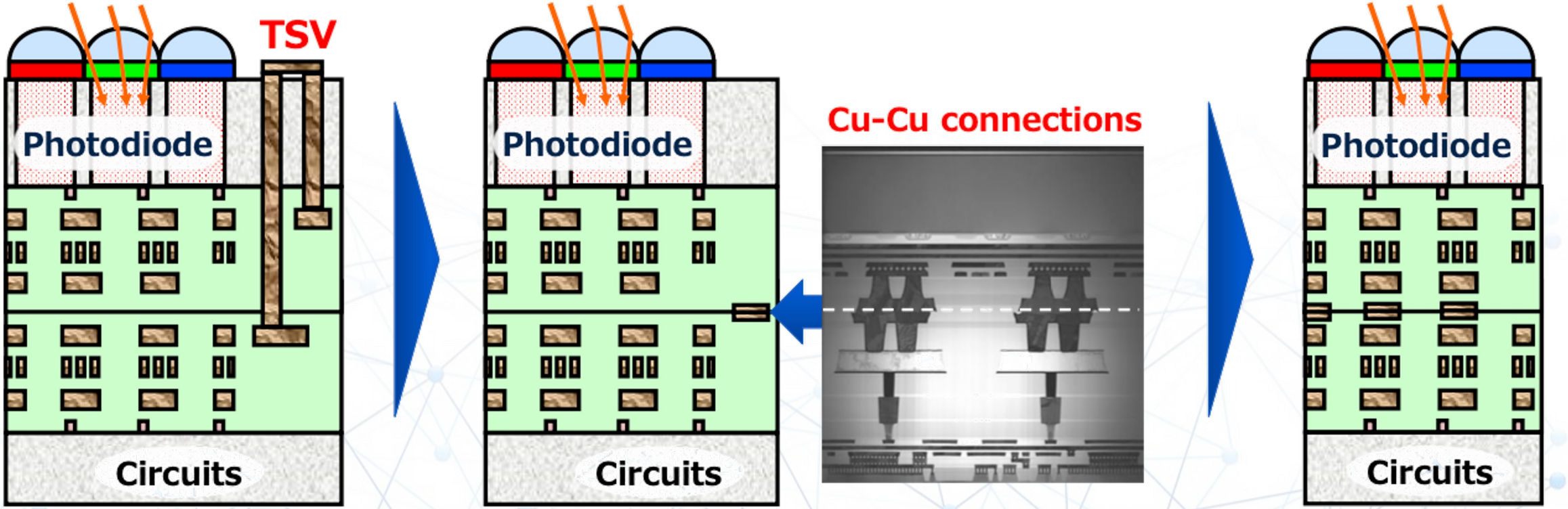




S. Sukegawa, ISSCC 2013

Hybrid Bonding Based CIS

- Cu–Cu connections have been introduced under pixel arrays



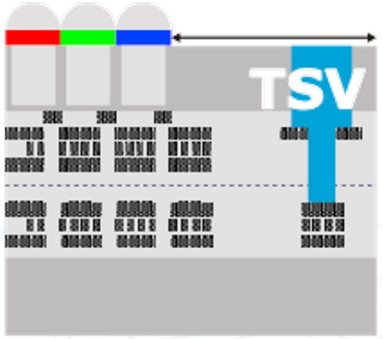
Y. Kagawa, IEDM 2016

Roadmap of 3D Stacking Sensors

- Pixel parallel architecture is becoming reality.

Device Structure

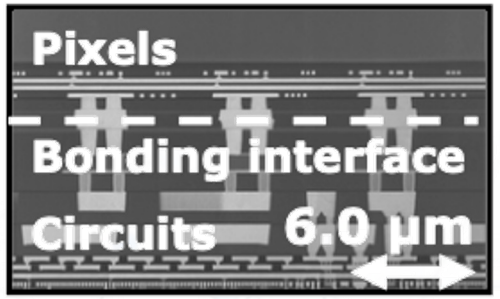
TSV Connection



Cu-Cu Connection

Y. Kagawa, IEDM 2016

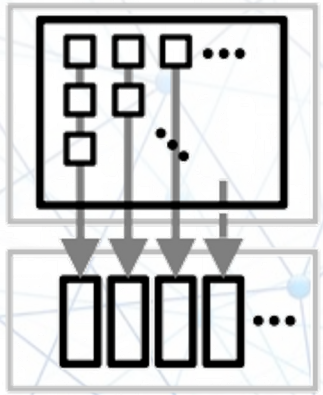
Pixel-level Connection



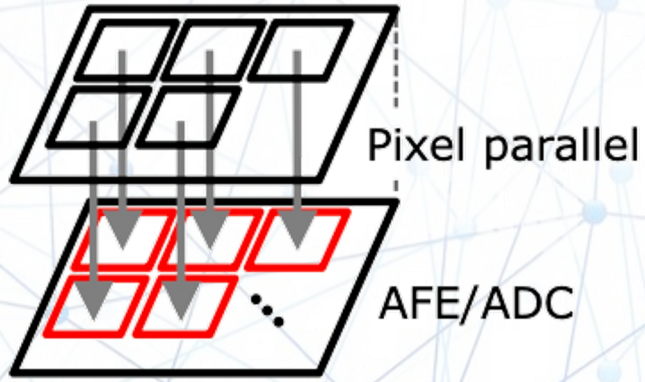
M. Sakakibara, ISSCC 2018

Readout Architecture

Column-parallel ADC

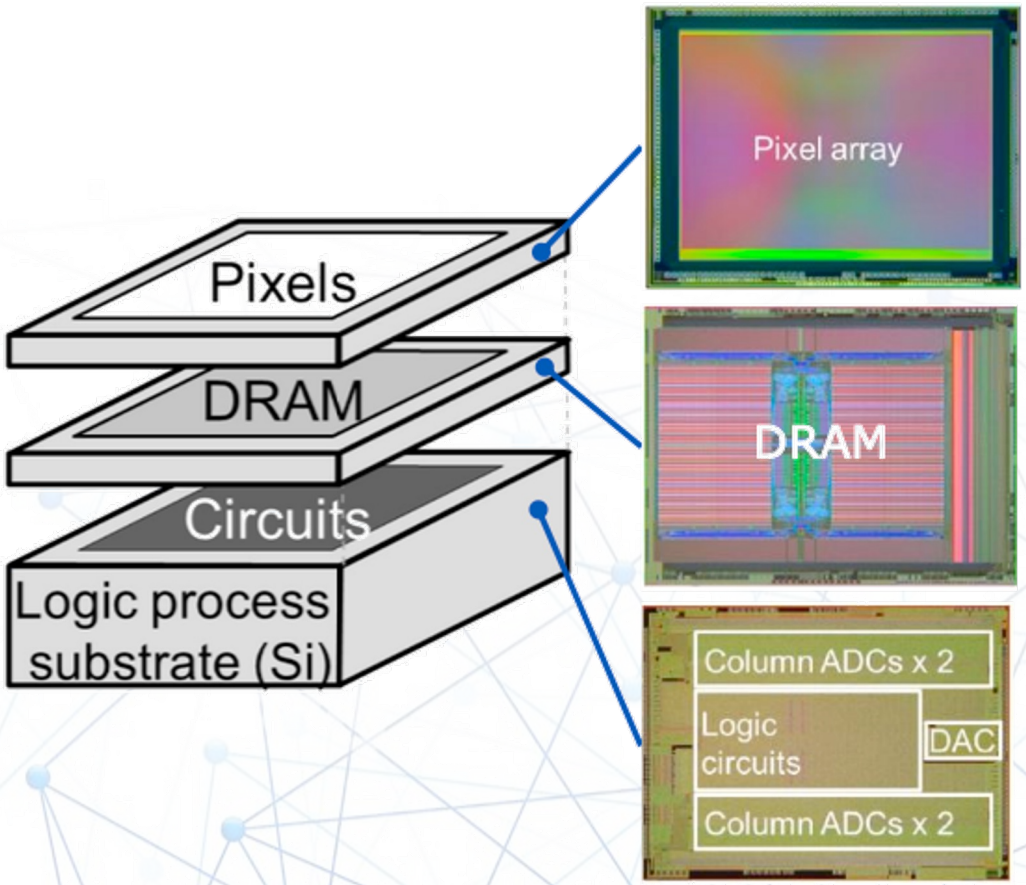


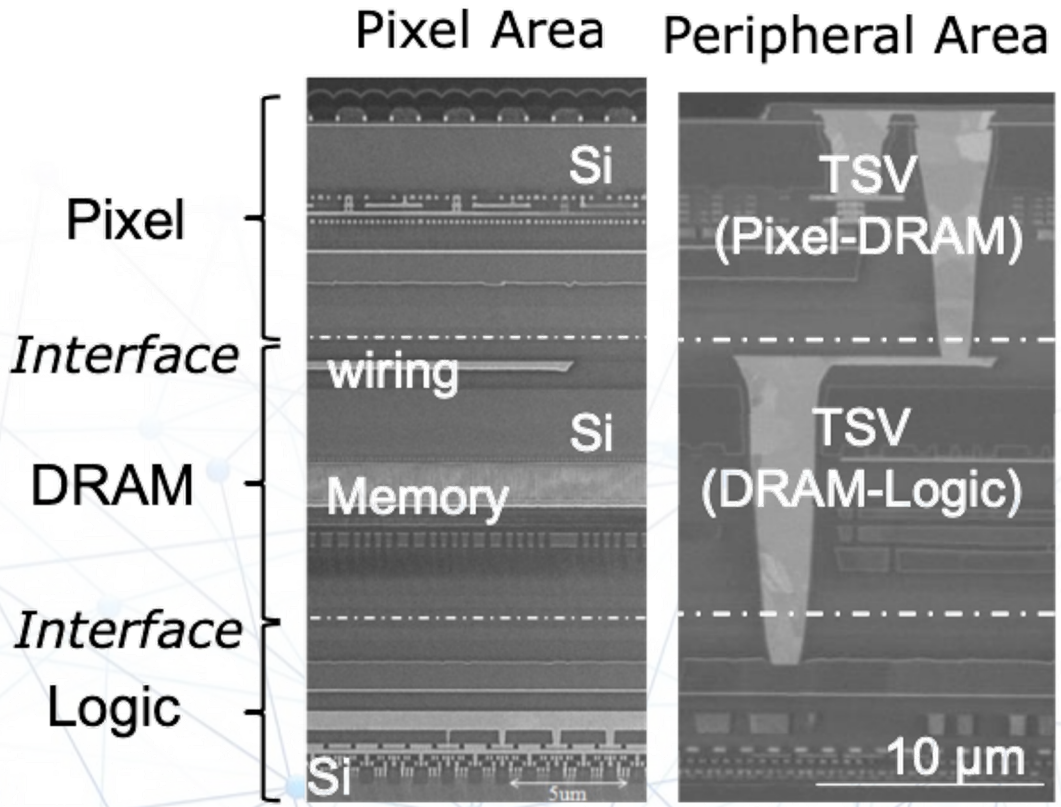
Pixel-level Digitization



Three Layer Stacked CIS with DRAM

- DRAM buffer having wide data bandwidth for slow-motion capture

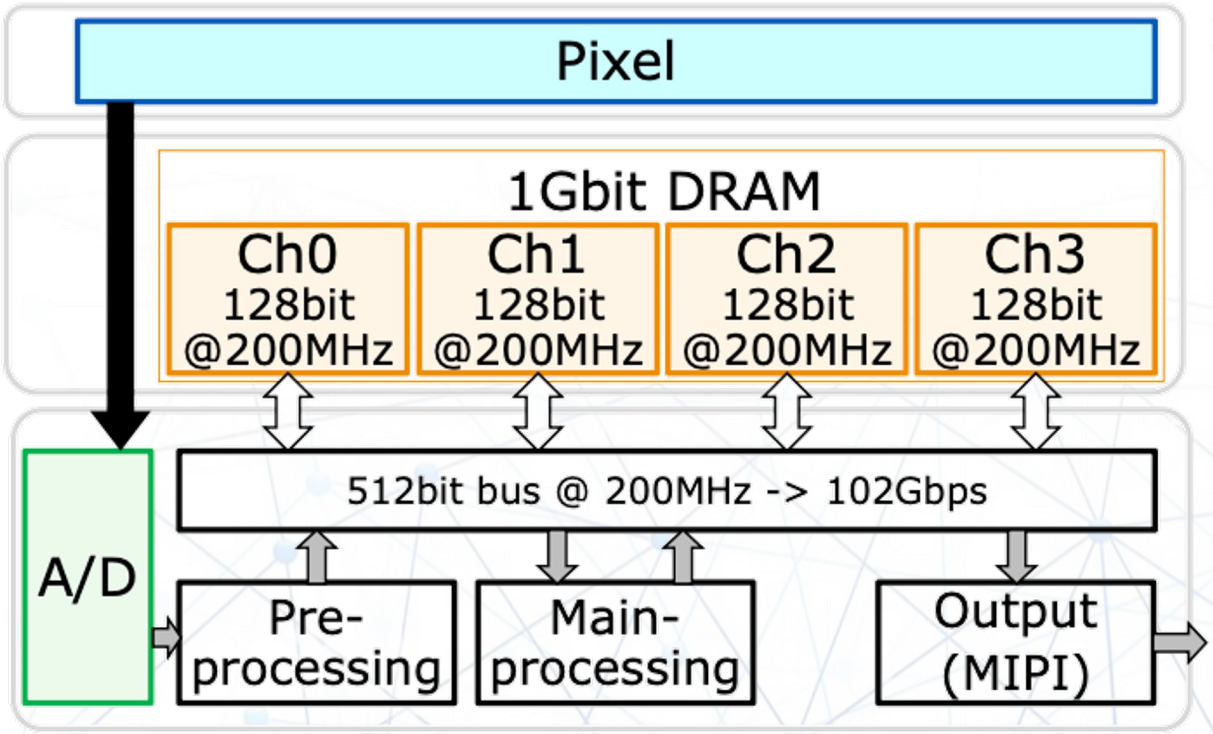


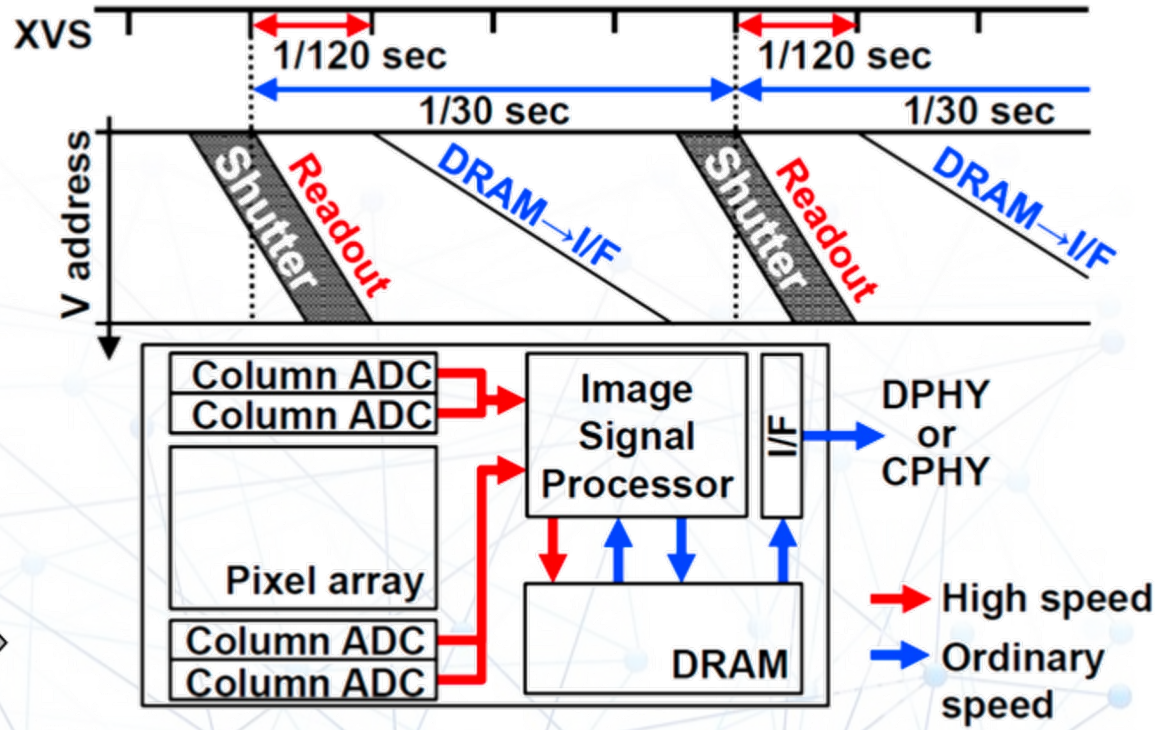


T. Haruta, ISSCC 2017
H. Tsugawa, IEDM 2017

Three Layer Stacked CIS with DRAM

- Enables slow-motion capture overcoming I/F limitation

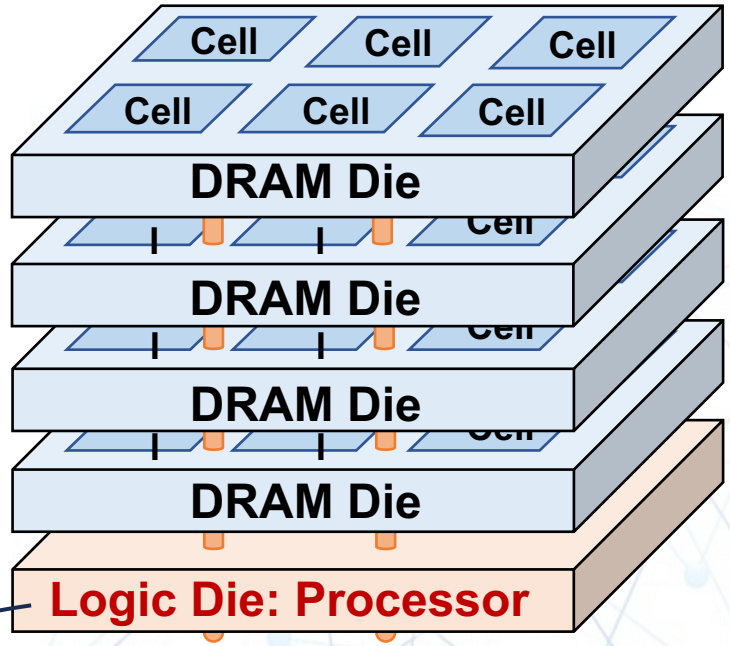




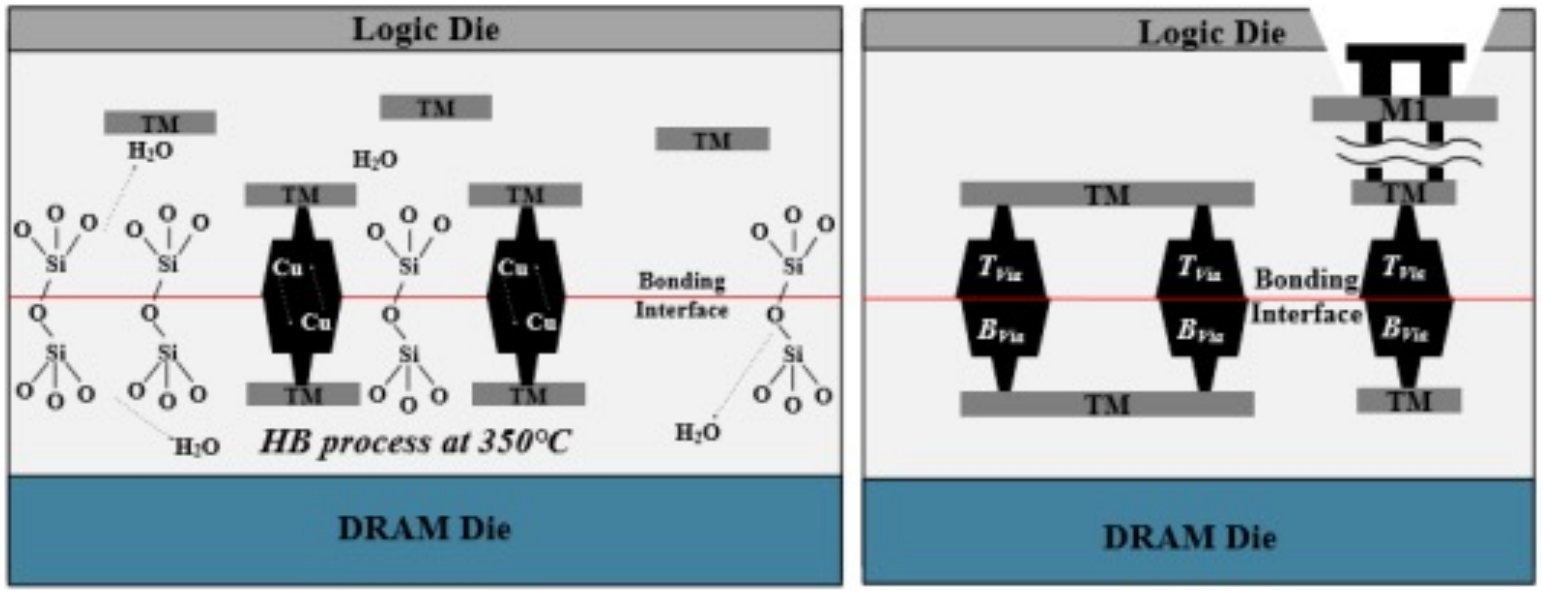
T. Haruta, ISSCC 2017

3D Stacking of Memory and Logic Die

➢Vertically 3D stacking memory die and logic die with hybrid bonding, which achieve high density interconnect and decoupling fabrication.



In contrast, HBM base die only has IO functions.

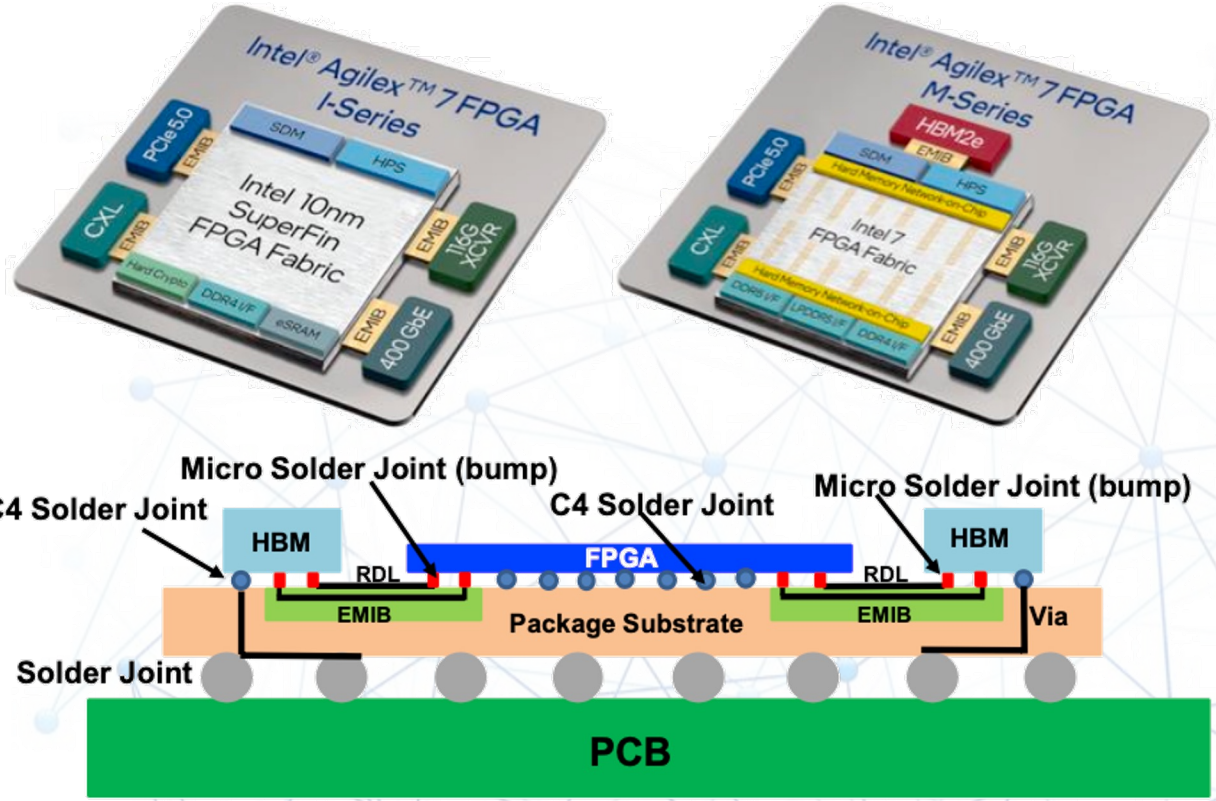


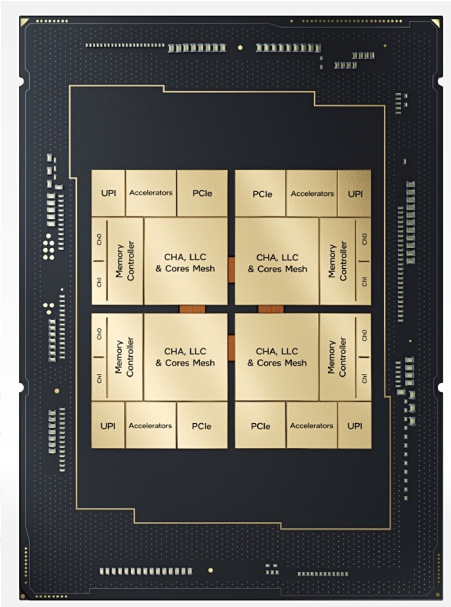
Cu-Cu Direct bonding with low temperature (300-350 ˚C)
Cu-bump pitch is ≤3μm, Effective bandwidth up-to-10TBps

[Alibaba Damo, ISSCC 2022]

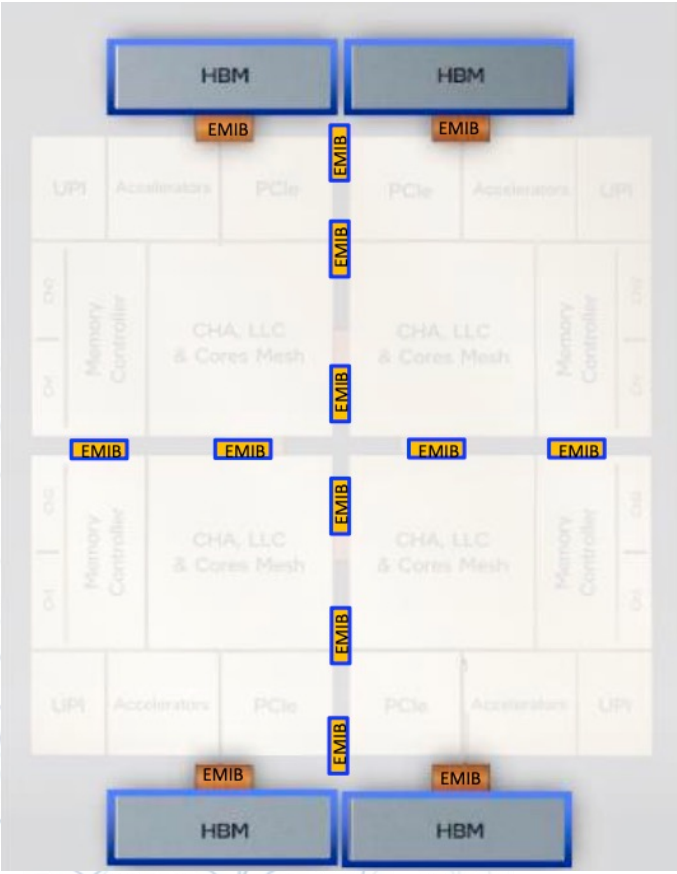
What is Silicon Bridges and Why?

- Large area silicon interposer with TSV has extremely high.
- High density interconnect only occurs in local and small area.

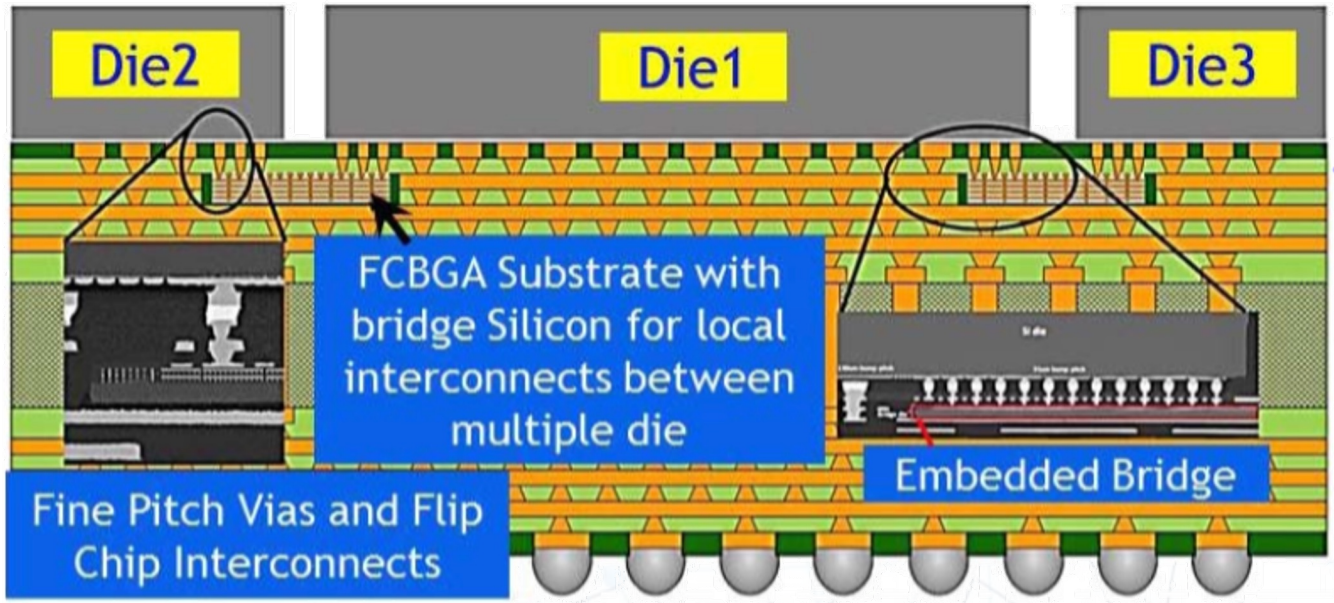


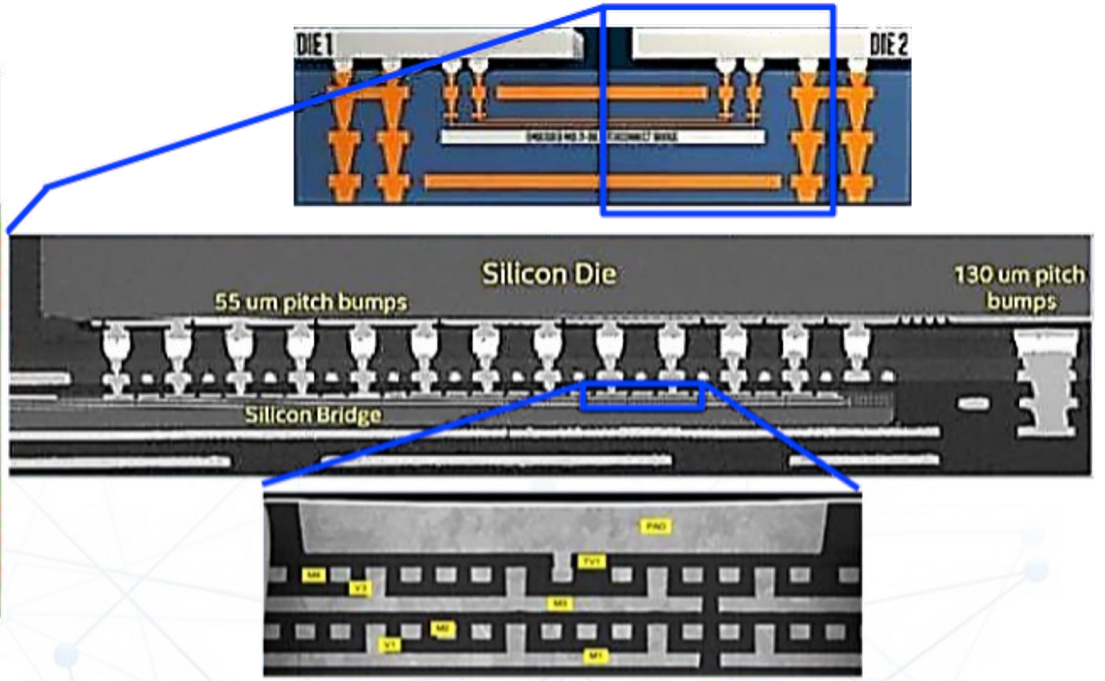


Sapphire Rapids
Intel Xeon 4th
Processor



Bridges Embedded in Substrate Process





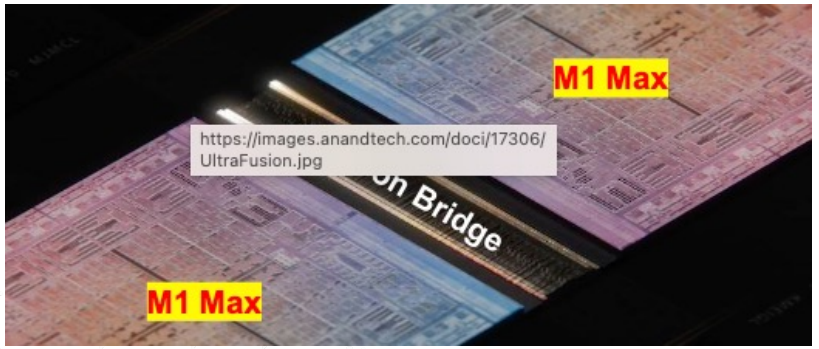
Source: Prismark (Intel EMIB 2020)

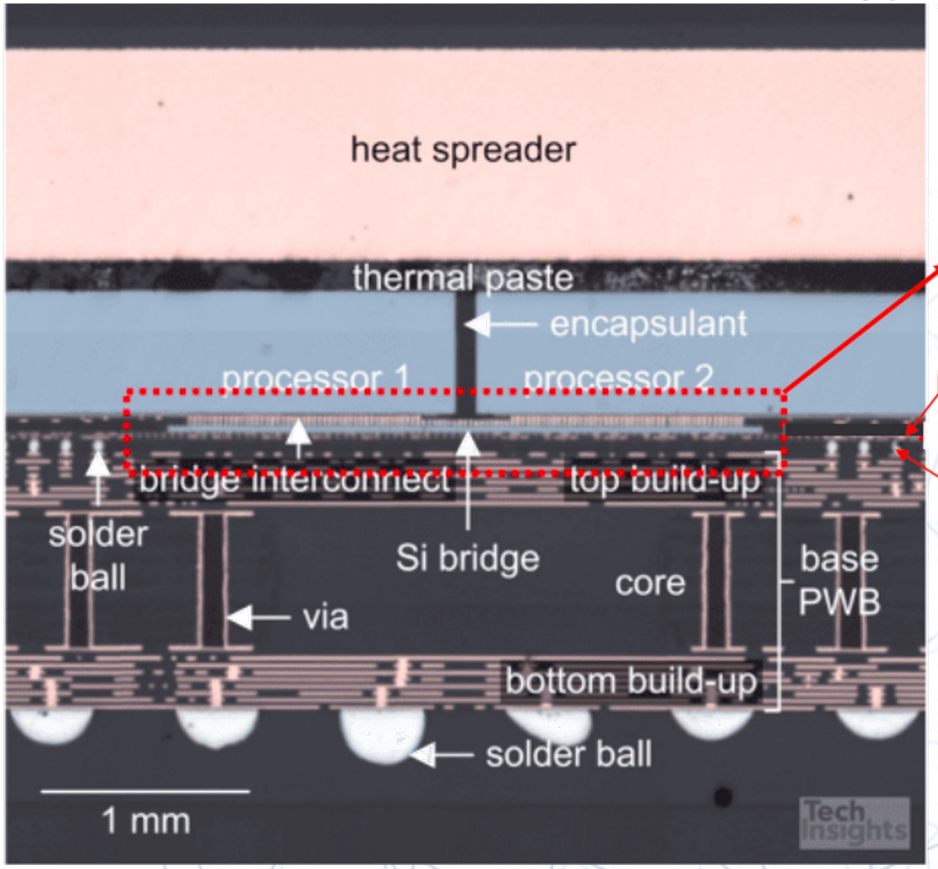
Process flow

Source: Ravi Mahajan, IEEE ECTC 2016, 557

Bridges Embedded in Epoxy Molding Compound

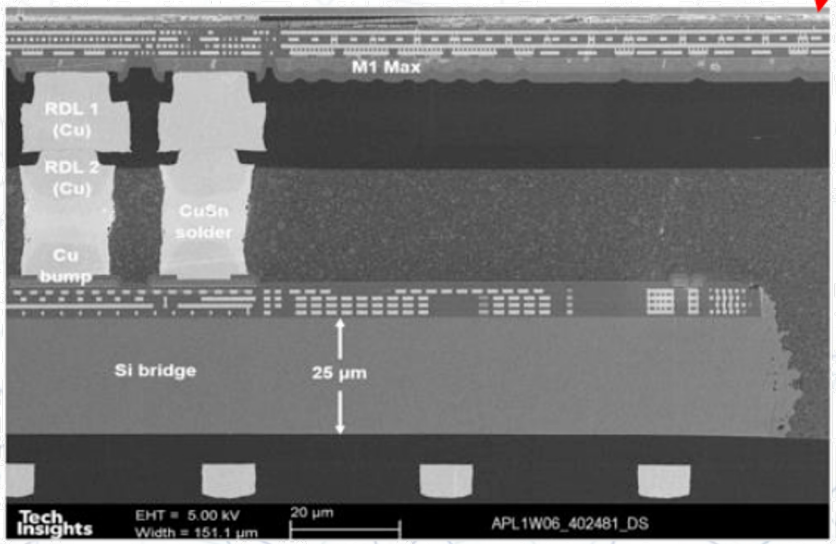
- FanOut technology use Epoxy molding compound (EMC) with RDLs, achieving 2μm line width
- Apple UltraFusion technology: 2xM1-Max = M1 Ultra

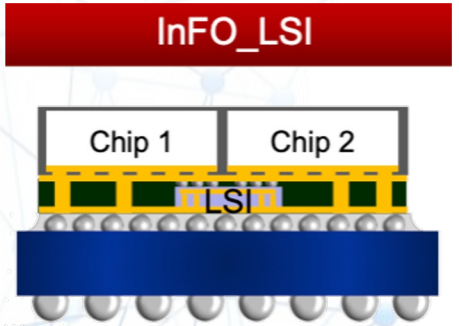




RDLs

C4 bump

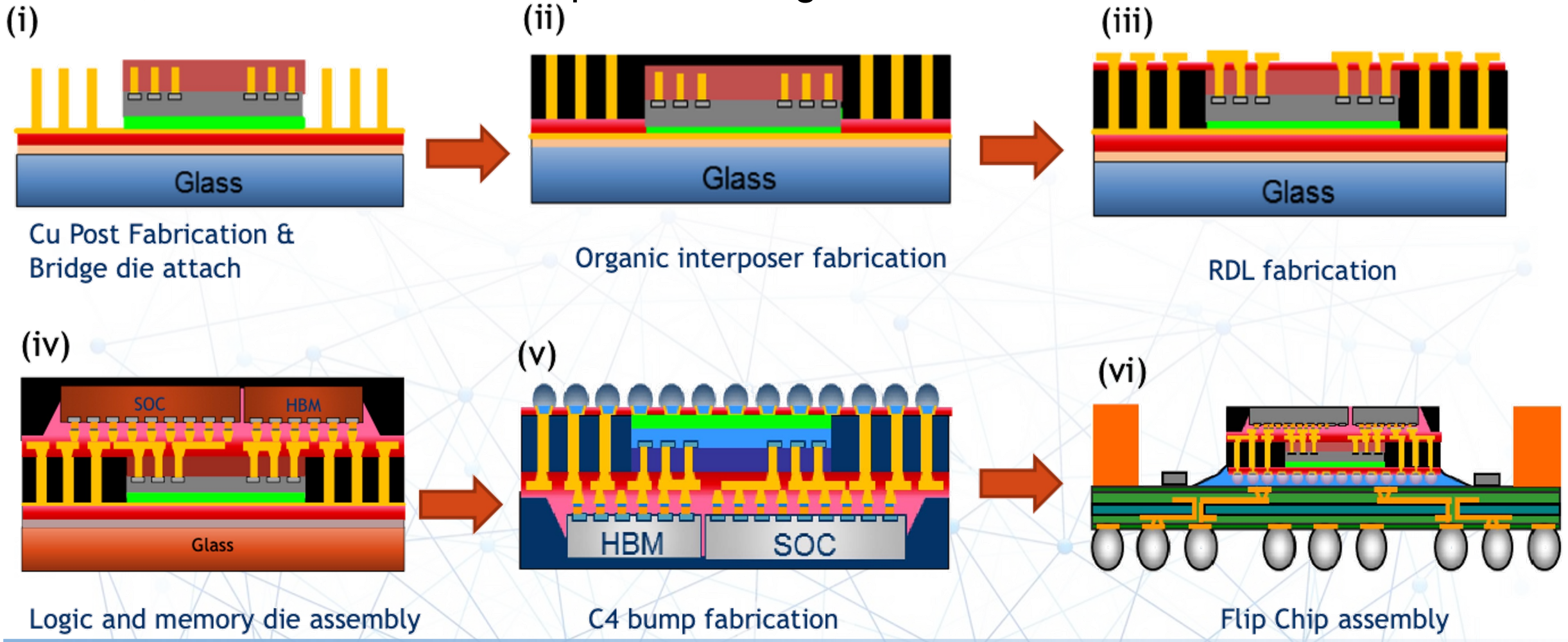




Originally called InFo-LSI
Now, CoWoS-L by TSMC

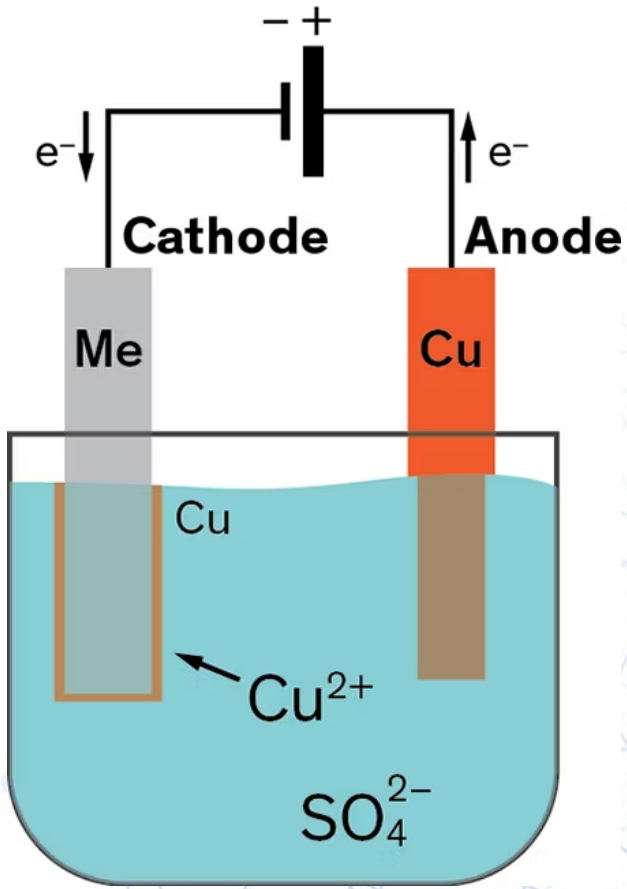
Fan-Out Embedded Bridge Process

- Cu pad/post are first built, and followed by molding and grinding to reveal post. Then, RDL fabrication and top die bonding.

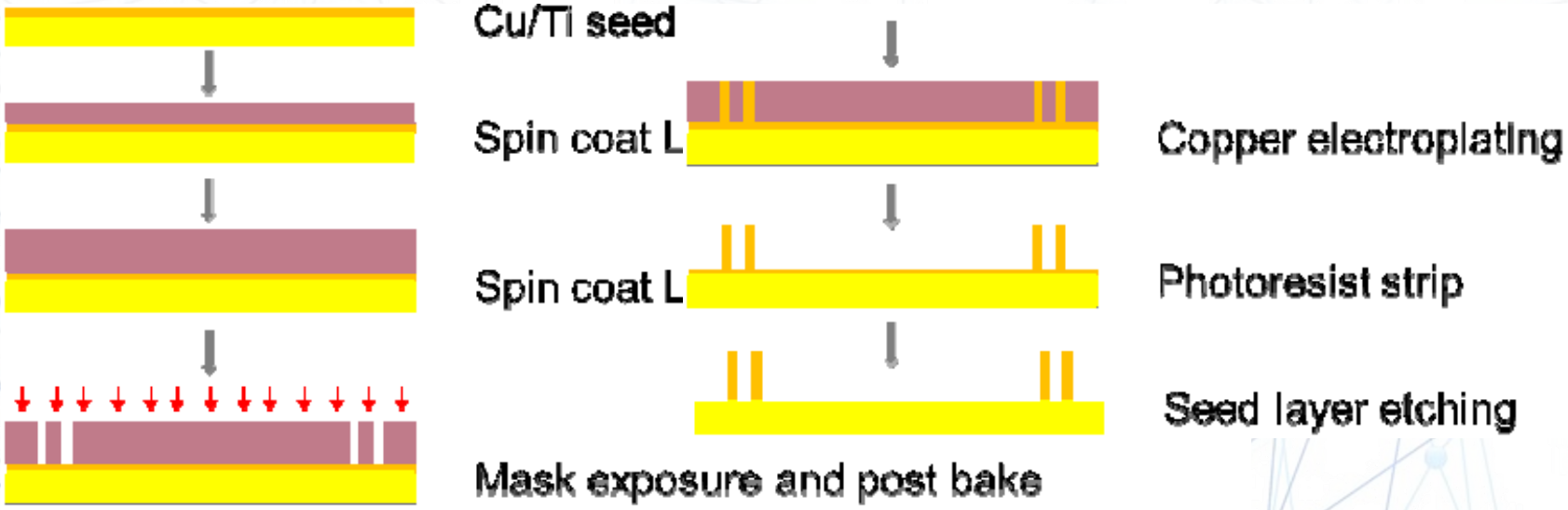


Cu Plating Bath

- In fan-out wafer-level packaging (FOWLP) technologies, copper posts are plated onto a temporary carrier before die attachment, resulting in a more simple way.



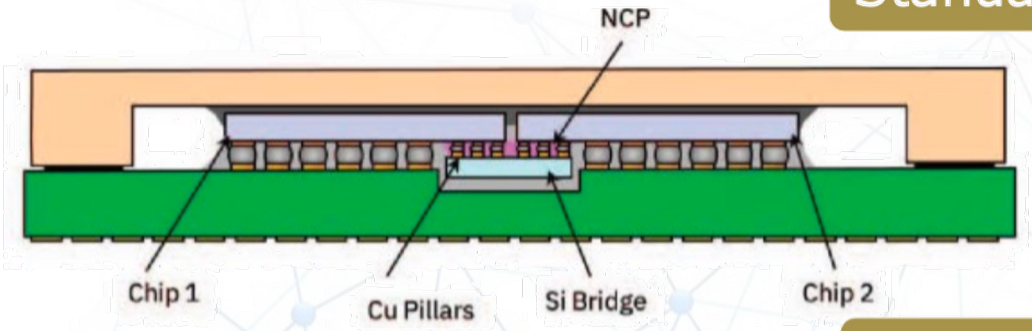
- A copper plating bath is an electrolyte solution used in the electroplating process to deposit a layer of copper onto a substrate.

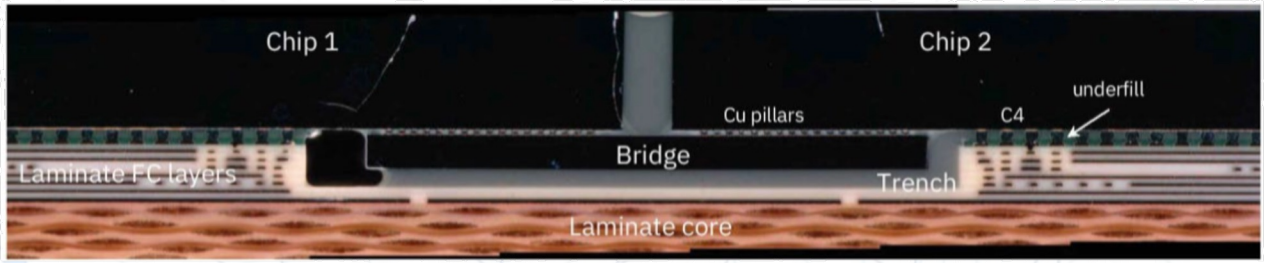


Silicon Bridge with Direct Bonded Tech

- Si bridge is directly bonded to and in between processor chips using Cu pillars.
- In standard DBHi package, a cavity is etched in the laminate substrate, while in surface DBHi, no cavity is etched in the laminate, but bridge die needs grindle.

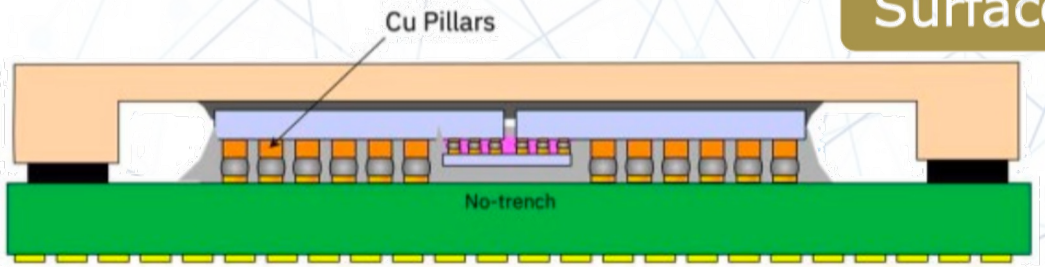
Standard DBHi Package





K. Sikka, ECTC, 2021

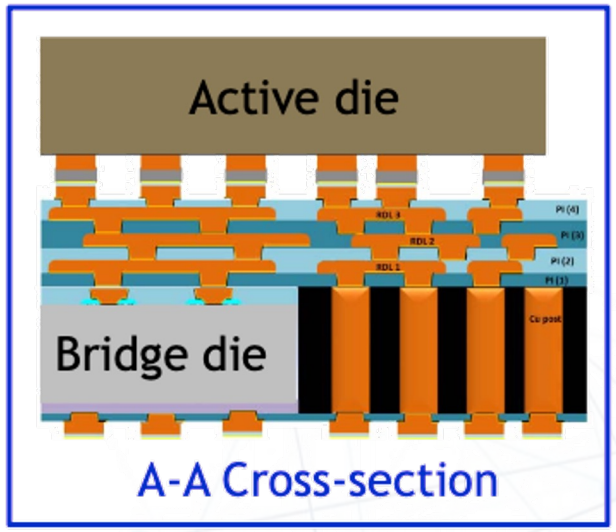
Surface DBHi Package

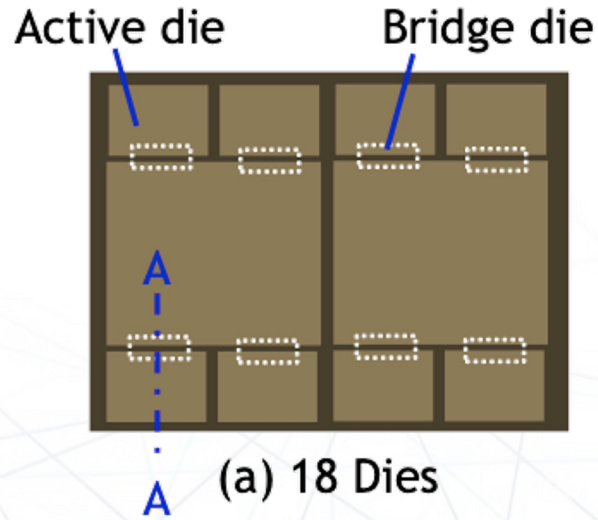


K. Sikka, EDTM, 2022

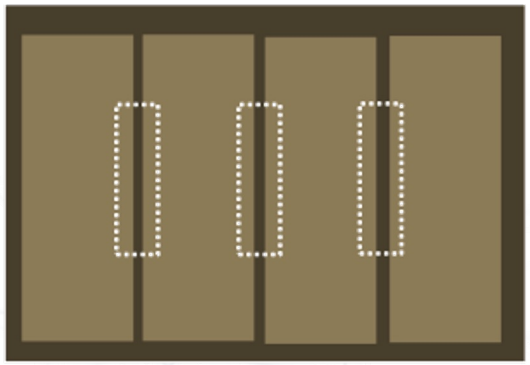
The good scalability of Fan-Out Bridge

- Molding compound can achieve large area much easier than Si-interposer.

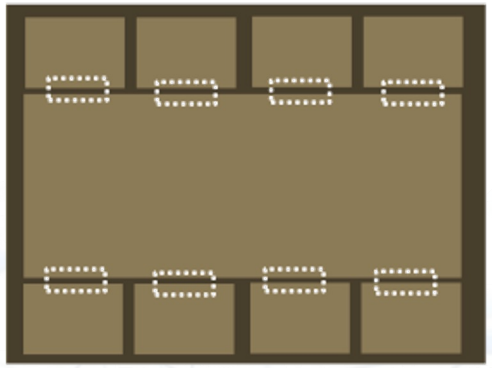




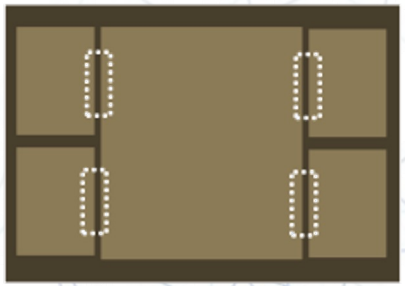
(a) 18 Dies



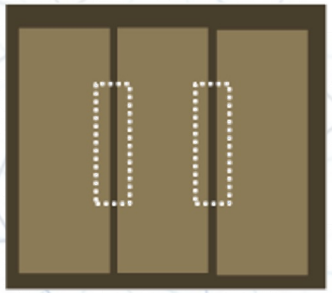
(b) 7 Dies



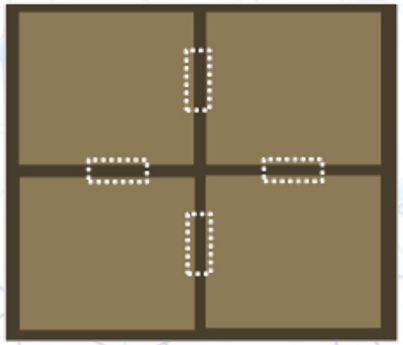
(c) 17 Dies



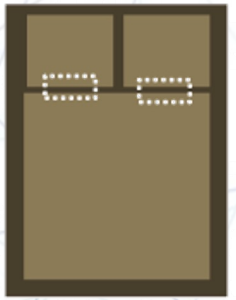
(d) 9 Dies



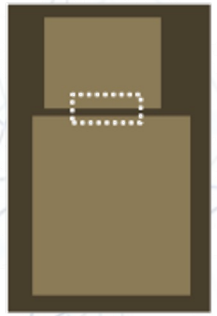
(e) 5 Dies



(f) 8 Dies



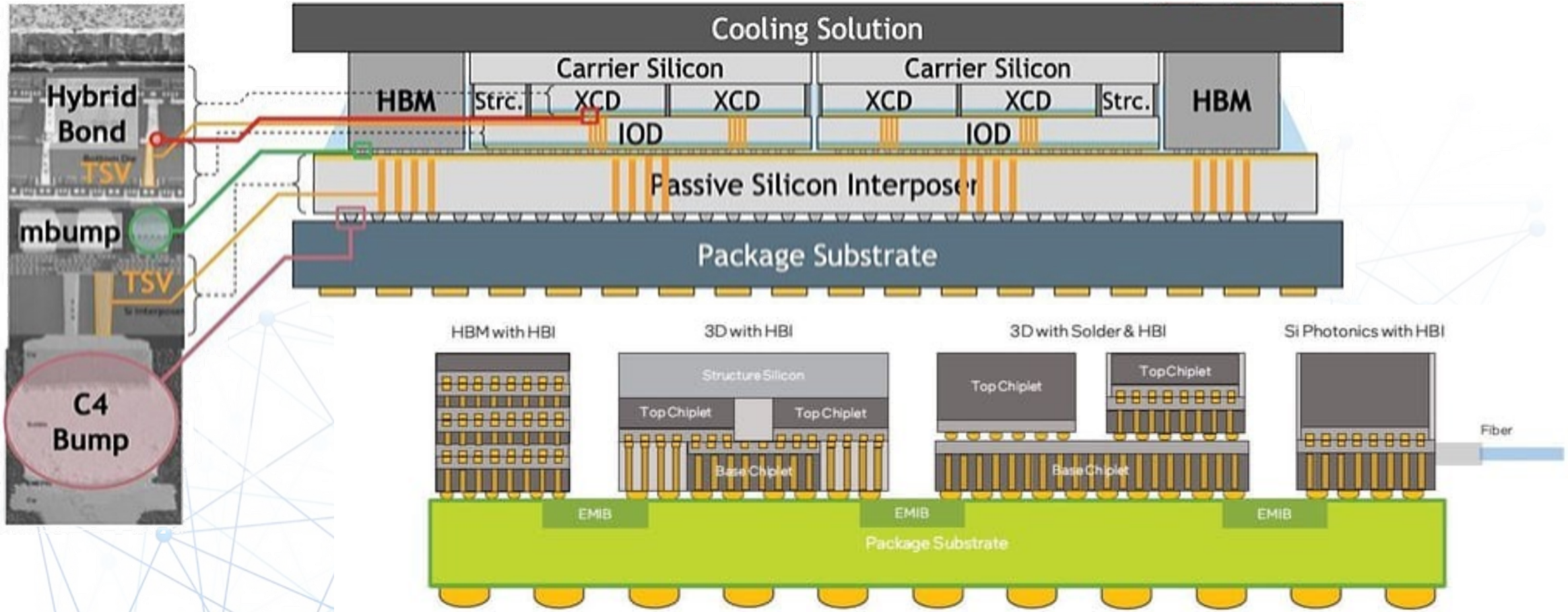
(g) 5 Dies



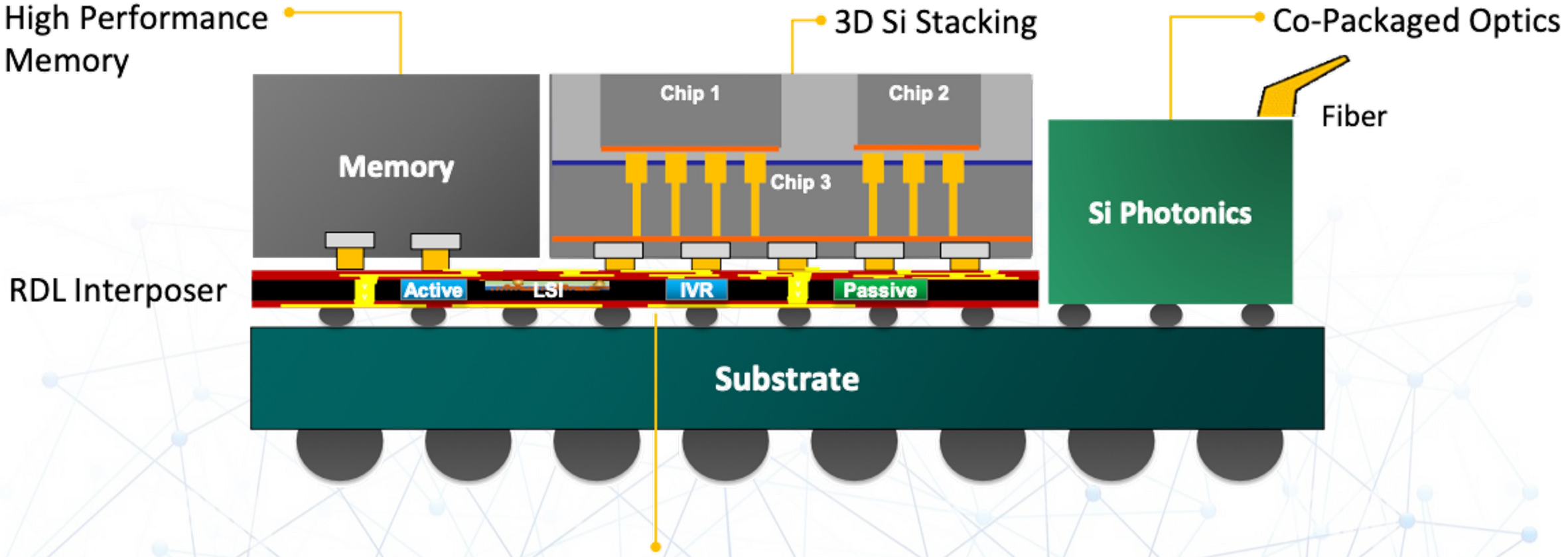
(h) 3 Dies

3.5D Integration for HPC

➢**3.5D** integration: hybrid approach that combines elements of both 2.5D and 3D packaging technologies, with vertical die stacking and interposer/bridge technology.

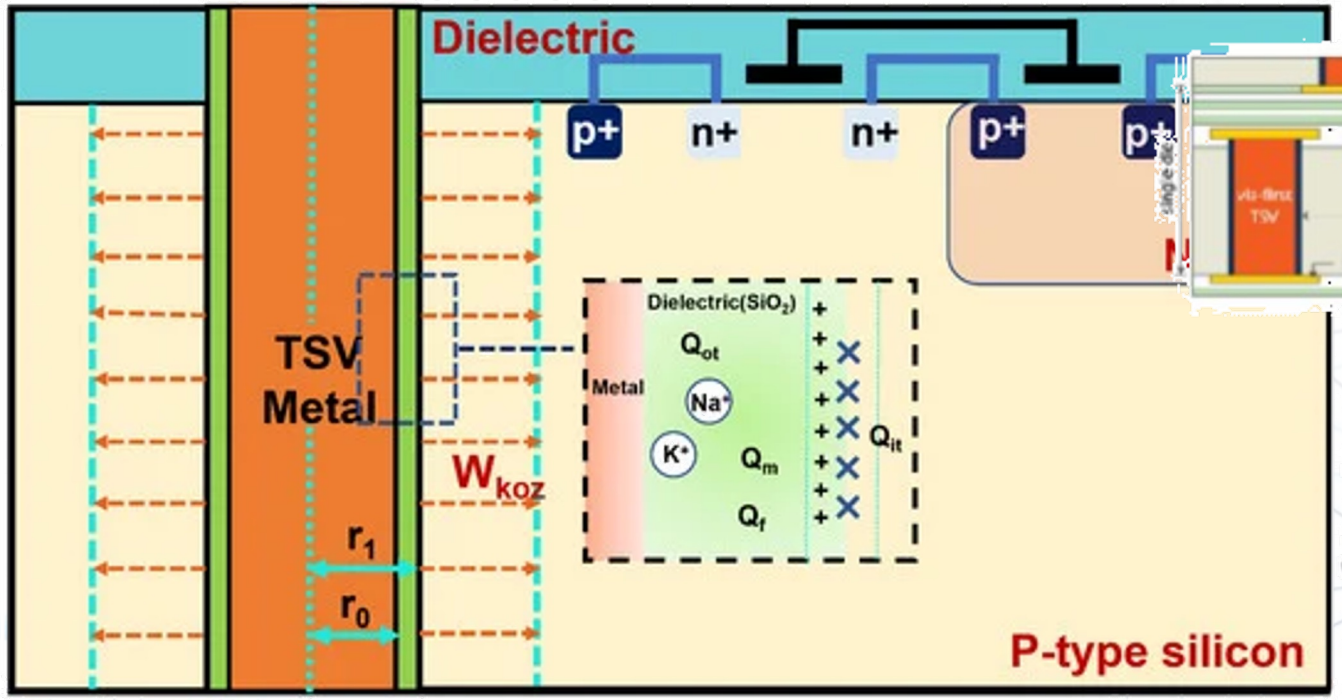


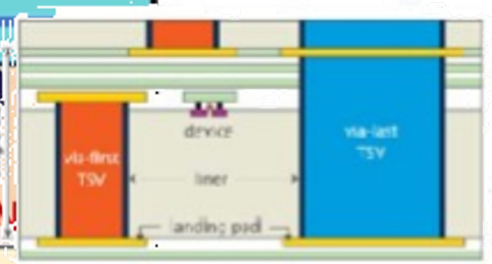
Future of the 3D AI Integrated System

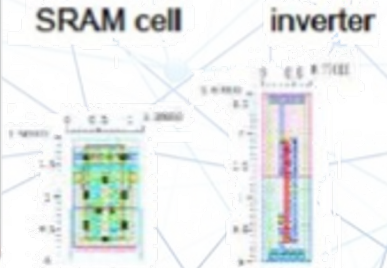


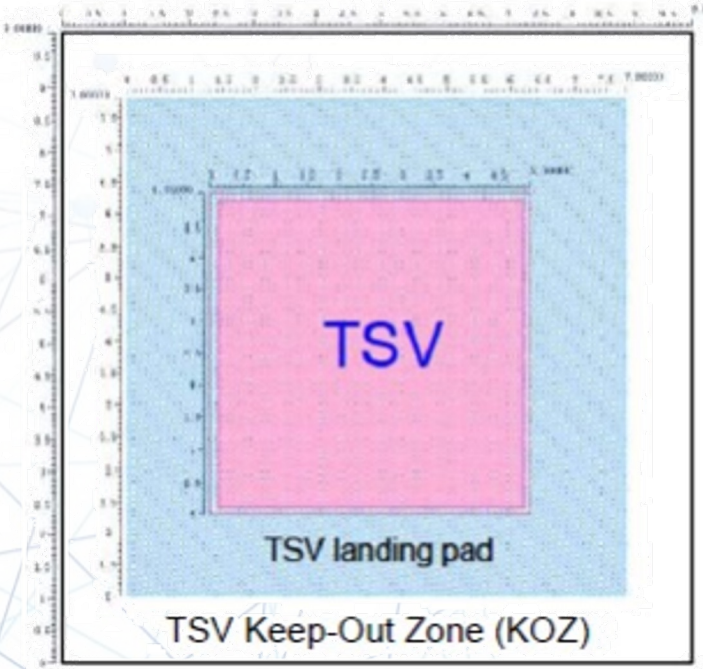
Design Consideration: TSV Keep-out Zone

- TSV keep-out zone (KOZ) refers to the area on a chip where devices cannot be placed near TSV, ensuring proper electrical isolation and structural integrity.
- Normally TSV KOZ is 5-10x higher than standard cel, with 10-20μm diameters.



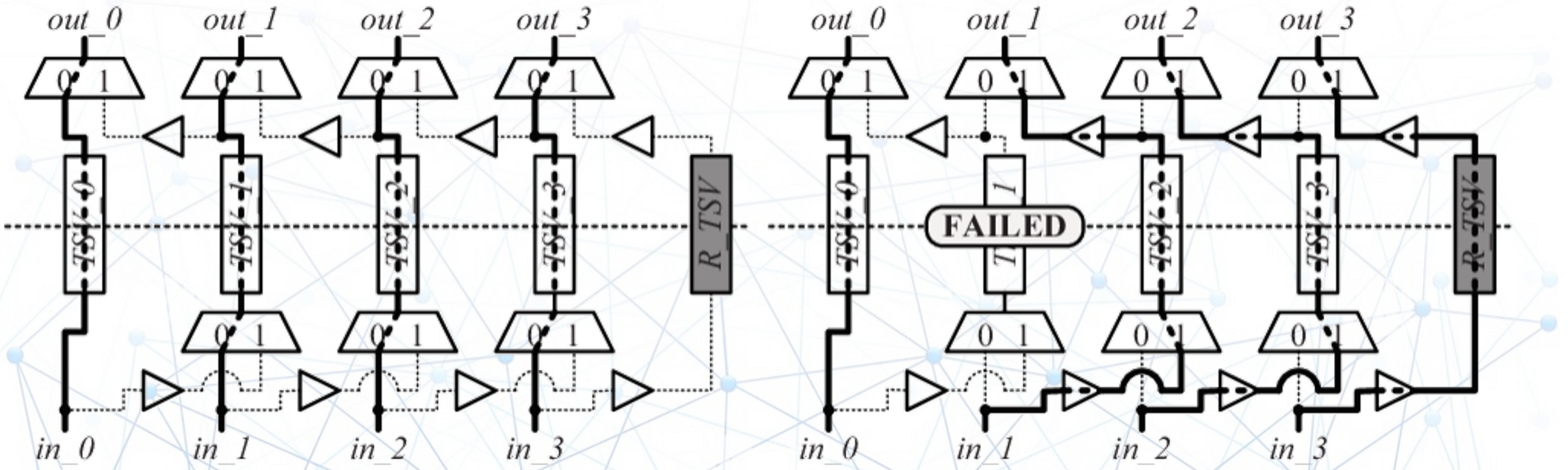






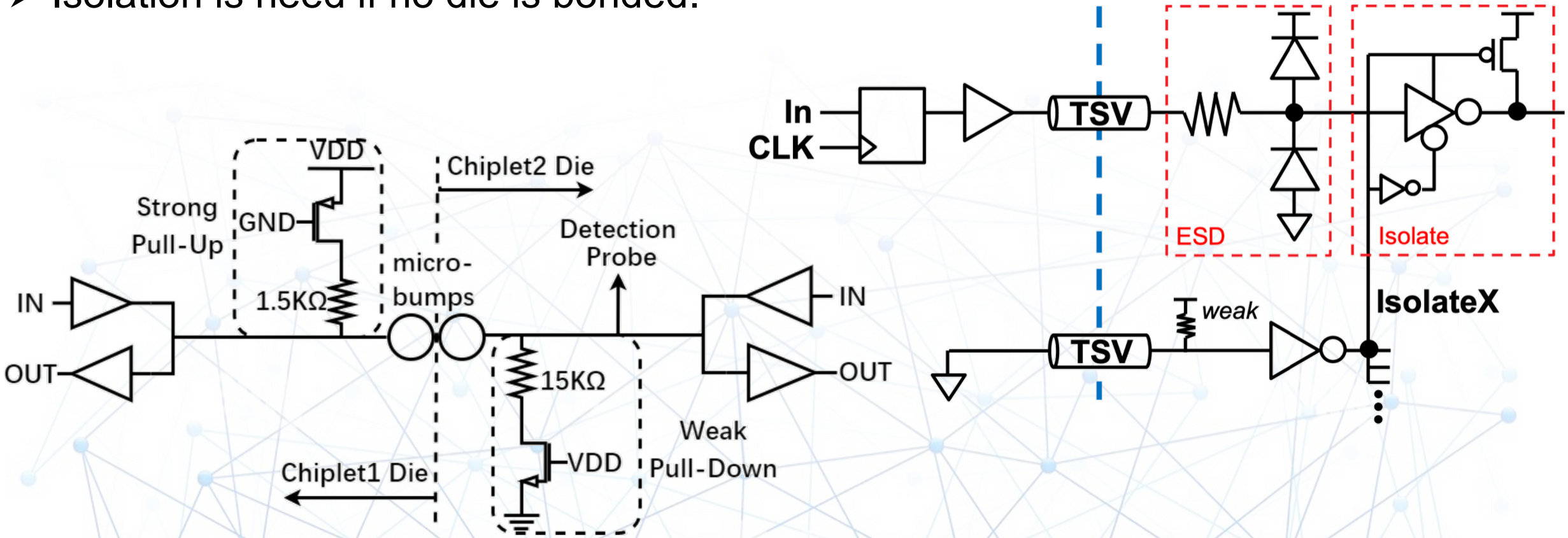
Design Consideration: μbump/TSV Redundancy

- Manufacturing defects can render some TSVs or micro-bumps non-functional, incorporating redundant devices allows the system to bypass these defective paths
- Once a failure is detected, a repair process involves shifting signals from the failed TSV to a functional one, ensuring continuous data transmission.



Design Consideration: μbump/TSV Redundancy

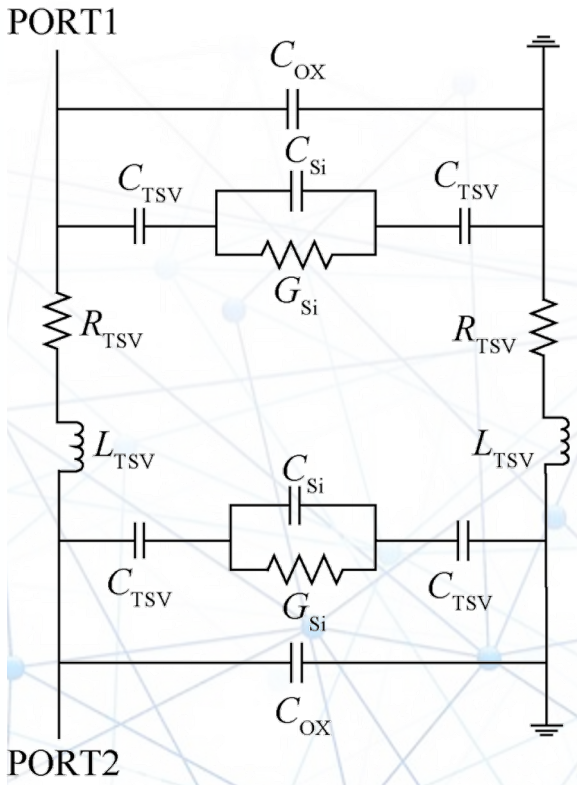
- Implement test structures and monitoring circuits to identify faulty TSVs. For example, voltage detectors are employed to verify their connectivity.
- Isolation is need if no die is bonded.

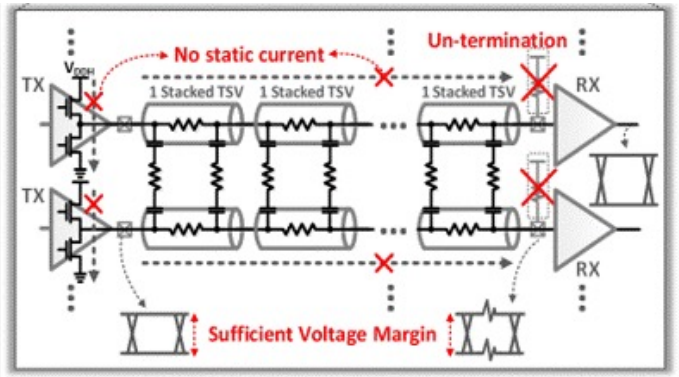


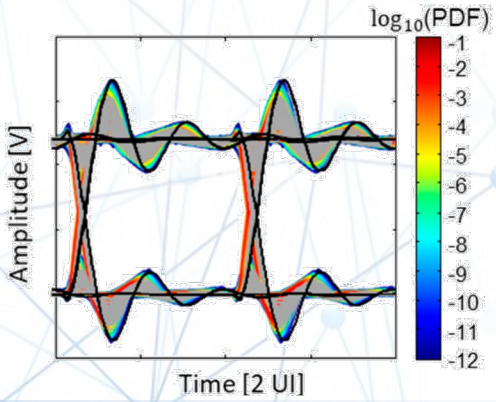
Design Consideration: TSV Max. Current

- TSVs in 3D IC have maximum current limits primarily due to electromigration, where high current densities cause the movement of metal atoms.
- TSV has EM effects and loss for highly switching of power delivery netorks.

Ref.	Akamatsu et al. ECTC 2016	This work
Structure	Conventional TSV structure with microbump	Bumpless TSV structure
Diameter	TSV (10 μm) IMC joint (30 μm)	TSV (10 μm)
Temperature	100 °C	200 °C
Current density	3.8×10^5 A/cm^2	7×10^5 A/cm^2
Criteria	10%	10%
MTF	4 hr	137 hr

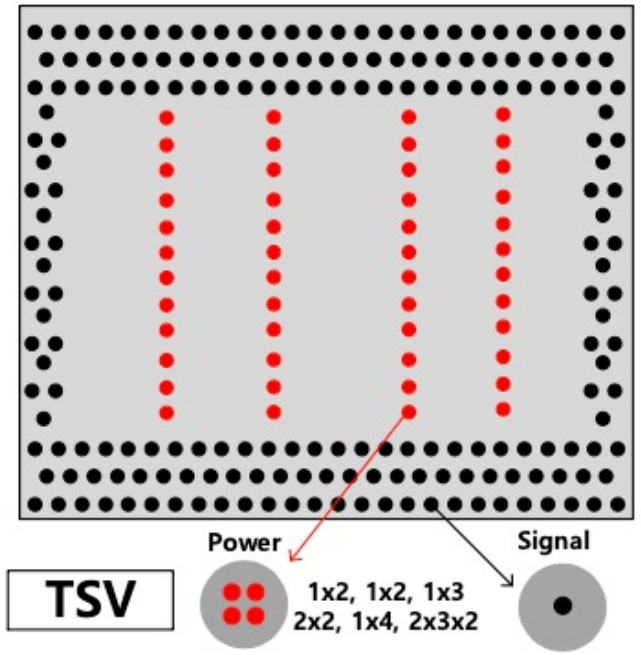




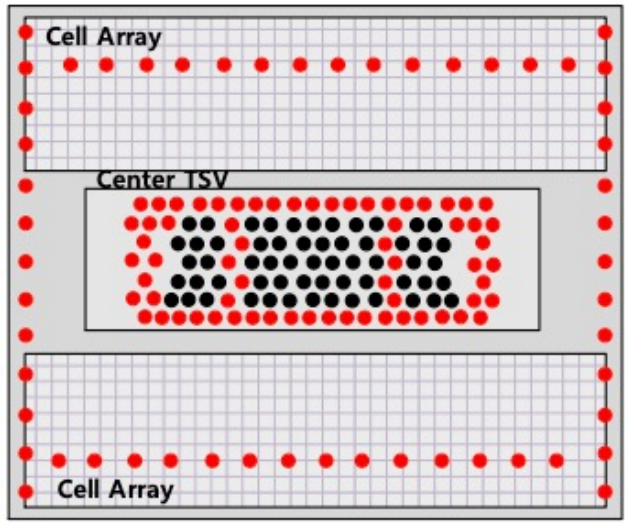


Design Consideration: TSV Placement

- TSV utilization for PDN improvement at 3D chip stacking
- TSV utilization cooperated with dedicated top power metal improved IR drop by 67%



[W. Gomes, ISSCC 2020]
3D Mobile System



[K. Chun, ISSCC 2020]
High Bandwidth Memory (HBM2E)