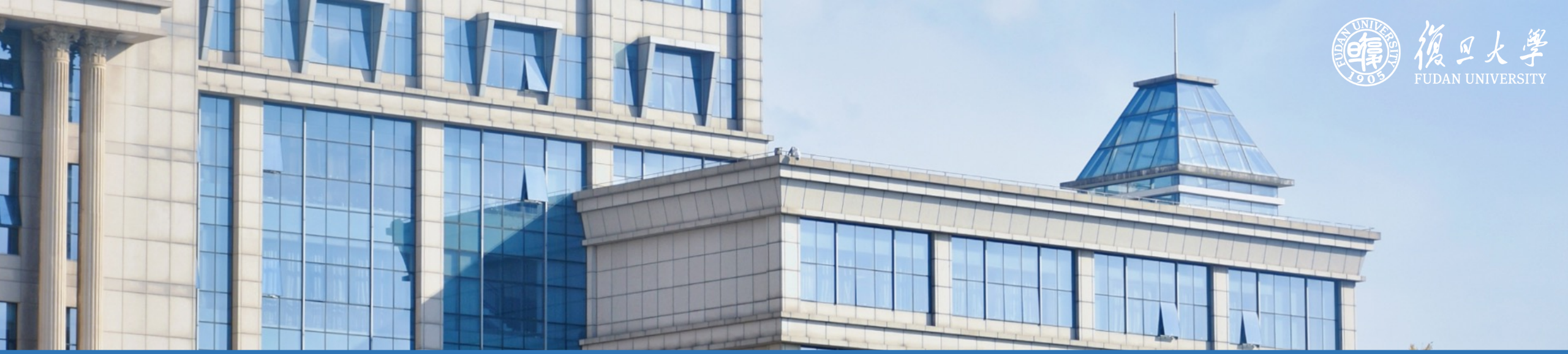


先进封装与集成芯片

Advanced Package and Integrated Chips

Lecture 3 : 3D Integration: TSV and HB

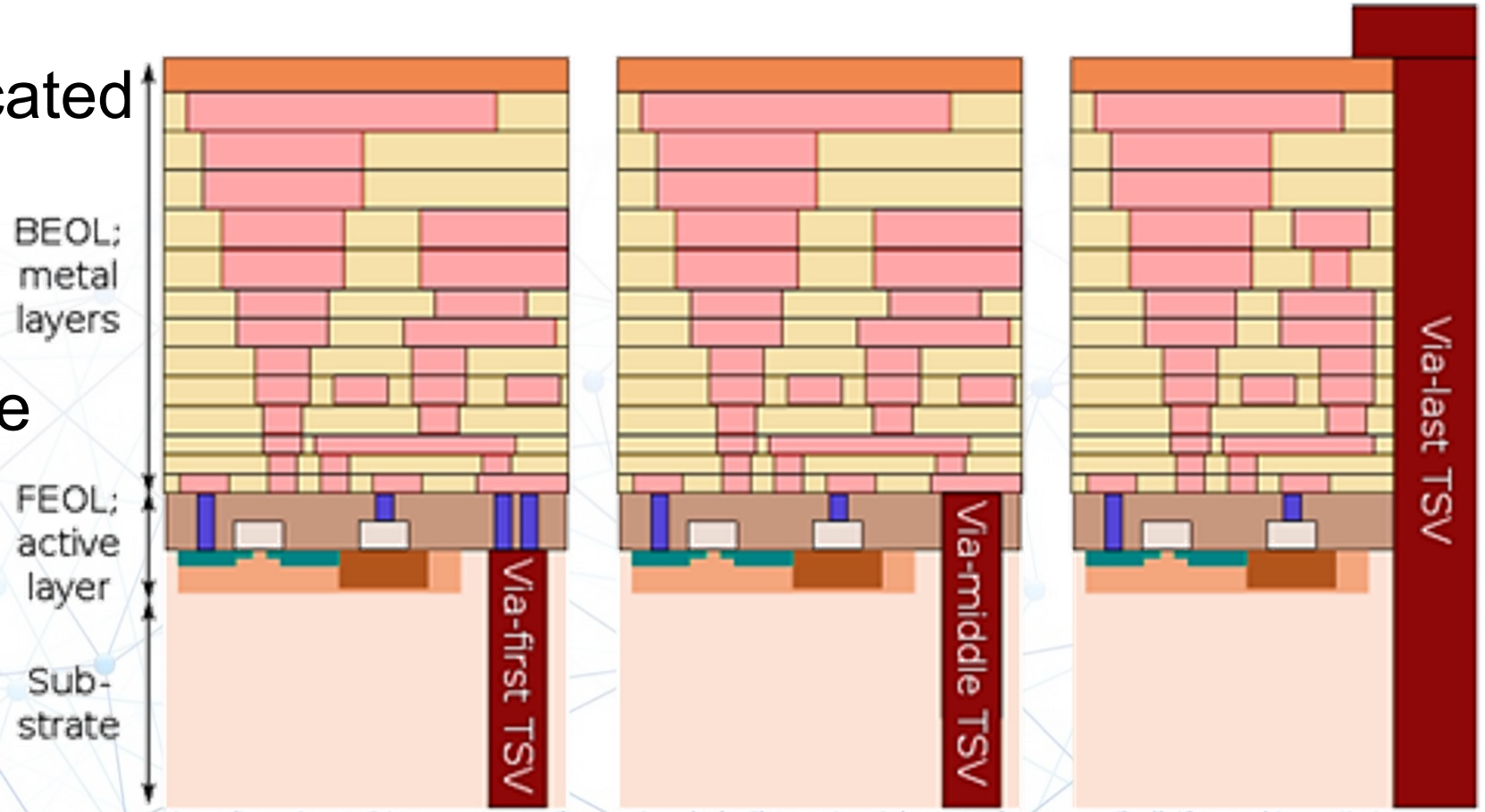
Instructor: Chixiao Chen, Ph. D

Overview

- TSV middle and last fabrication
- Hybrid Bonding
- 3D Stacking Technology in Commercial Products
  - 3D Stacking Memories (HBM)
  - 3D Stacking Sensors

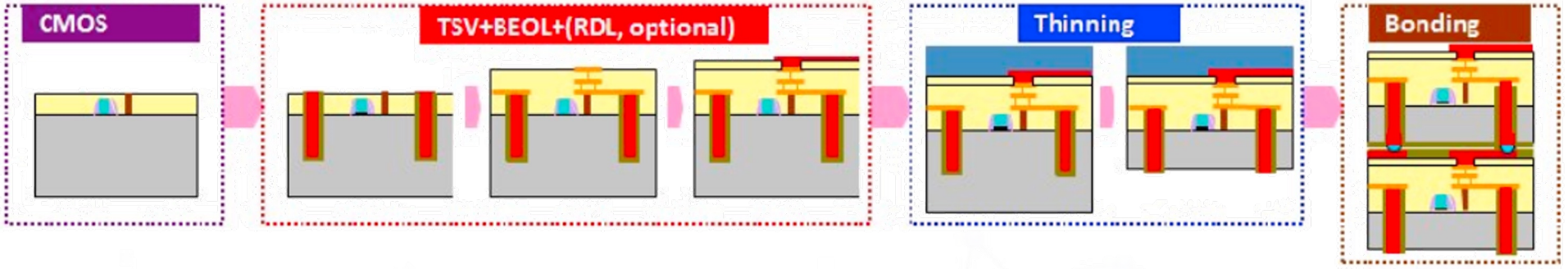
Via-first Via-Last and Via-Middle

- Through silicon via is the via in a piece of silicon letting the signals from the topside to the bottom-side or vice versa.
- Via-first: TSV fabricated before transistors
- Via-middle: after transistors but before metal completes
- Via-last: after wafer is fabricated



TSV fabrication Process flow

(1) Via-middle process flow

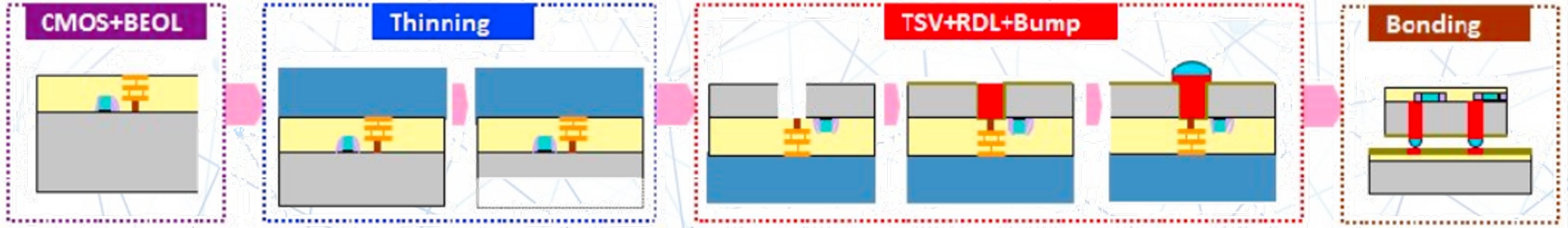


TSV revealing and routing issue
Only available in semiconductor fab

(2) Frontside via-last process flow

Not easy to implement high aspect ratio TSV
Can be implemented in OSAT

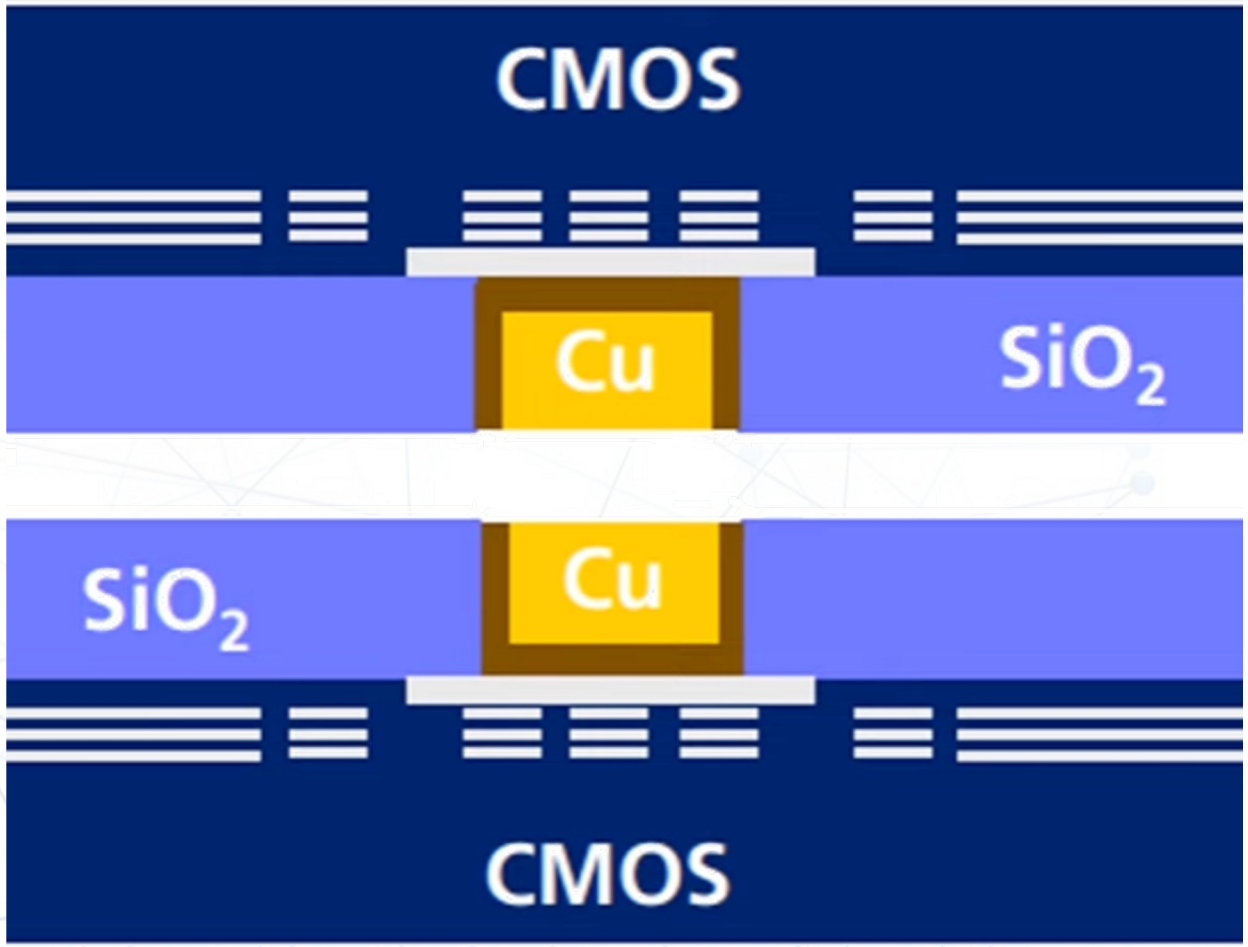
(3) Backside via-last process flow



No limitation for routing rules.

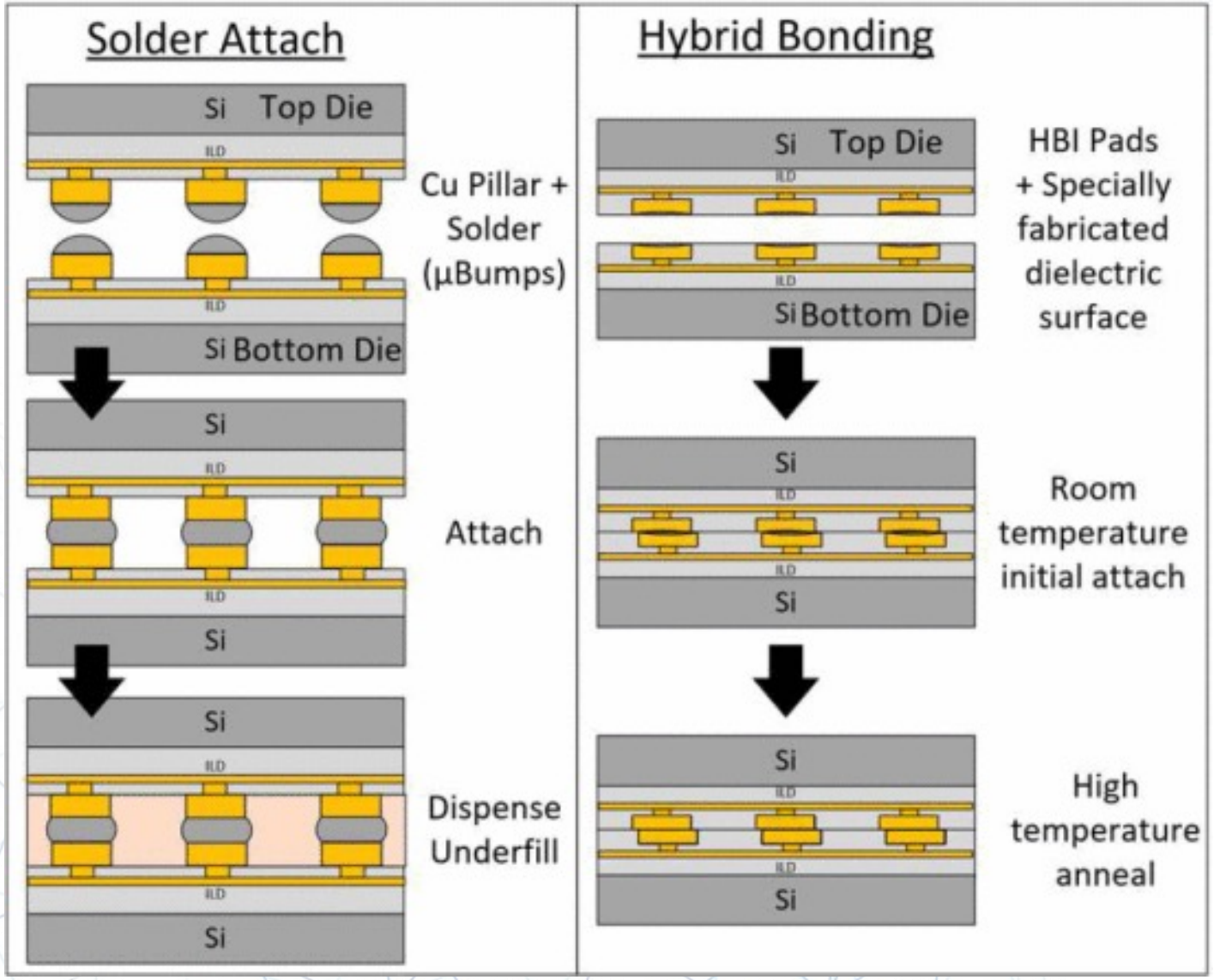
What is Hybrid Bonding ?

- Hybrid bonding (HB) is a dielectric bond combined with a metal bond to form an interconnection.
- Effectively replaces the Under Bump Metallization (UBM), underfill and micro-bumps with a direct connection.
- HB has much higher density than solder bumping technology.
- HB involves D2W or W2W processing at low temperature (<300 C) to initial high bond strengths.



Hybrid Bonding Process

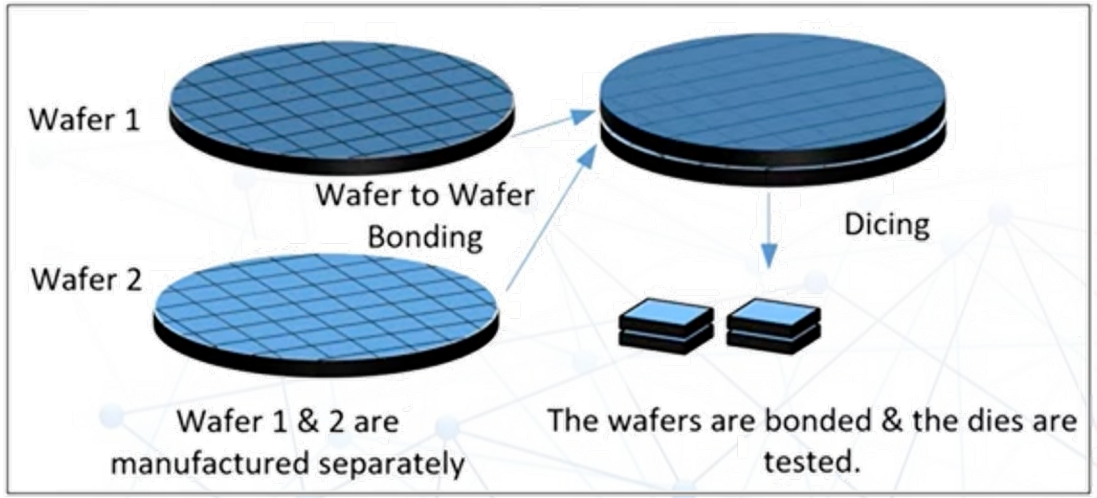
- Benefits:
  - Scalable pitch
  - 10x+ density over solder
  - Improved current carrying capability
  - Better thermomechanical performance
- Challenges:
  - Processing & Assembly
  - Test



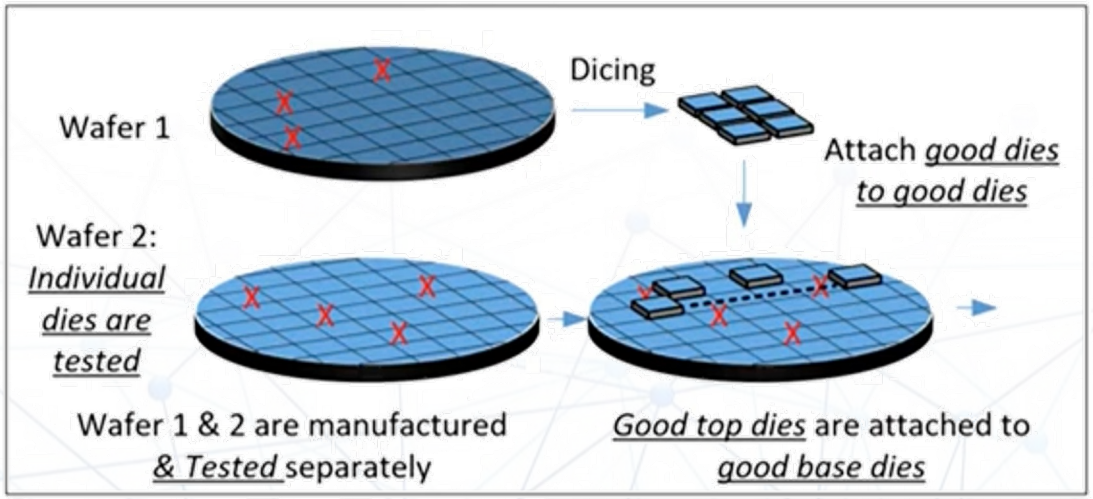
Two Types of Hybrid Bonding

- From design perspective, W2W HB requires same die area for both top and bottom chiplets.

Wafer to Wafer

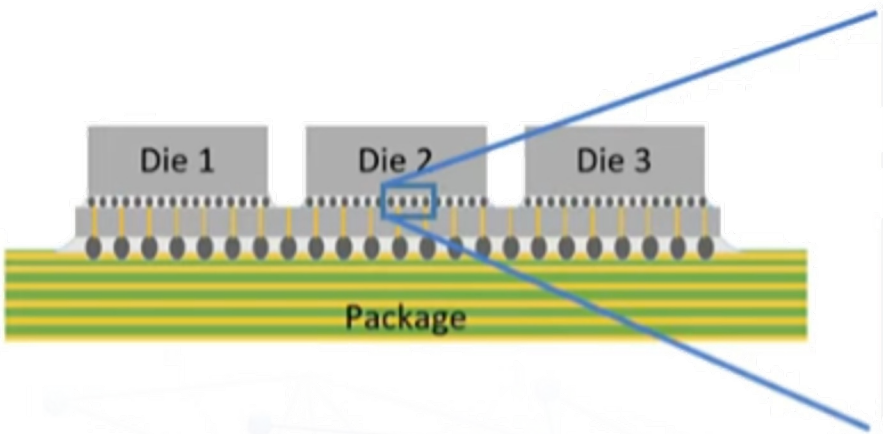


Die to Wafer

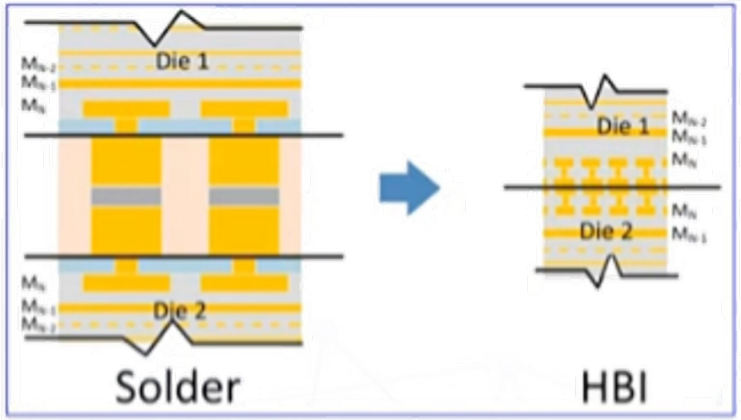


More mature	Less mature
Currently finer pitch	Currently coarser pitch with roadmap to finer pitch
Stacked dies must be the same size	No limitations on stacked die relative sizes
Each “layer” in the stack is a single technology	Can have top dies from different technologies
Cumulative yield issue (both dies must work)	No cumulative yield (top & bottom are tested before attach)

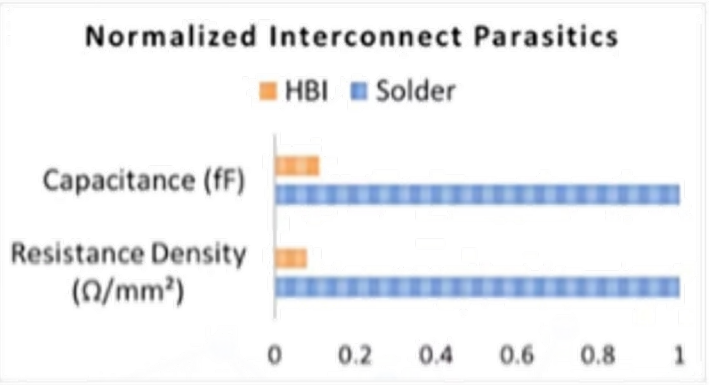
Hybrid Bonding Interconnect Parasitic



Solder Interposer Package



Die to die Interface



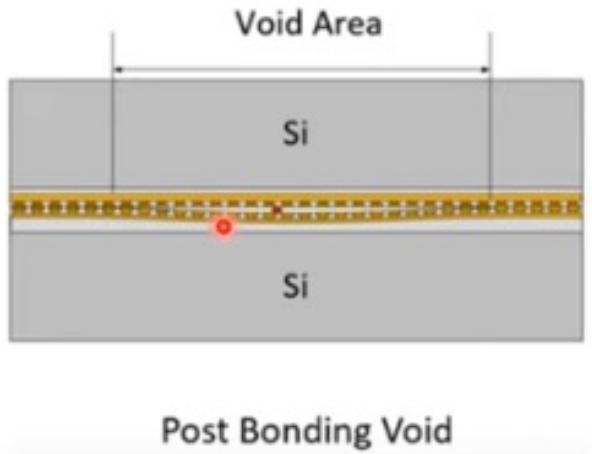
Parasitics Reduction

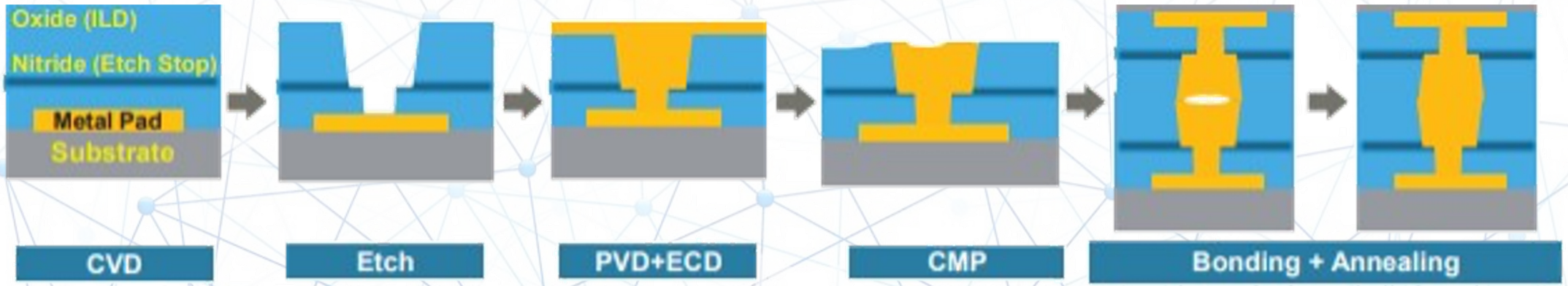
- Hybrid bonding pads area & height << solder microbumps
- Enables improved resistance and capacitance
- However, need to consider drivers & other circuitry(*)

(*) A. Elsherbini et al, "Hybrid Bonding Interconnect for Advanced Heterogeneously Integrated Processors," *2021 (ECTC)*

Surface Preparation

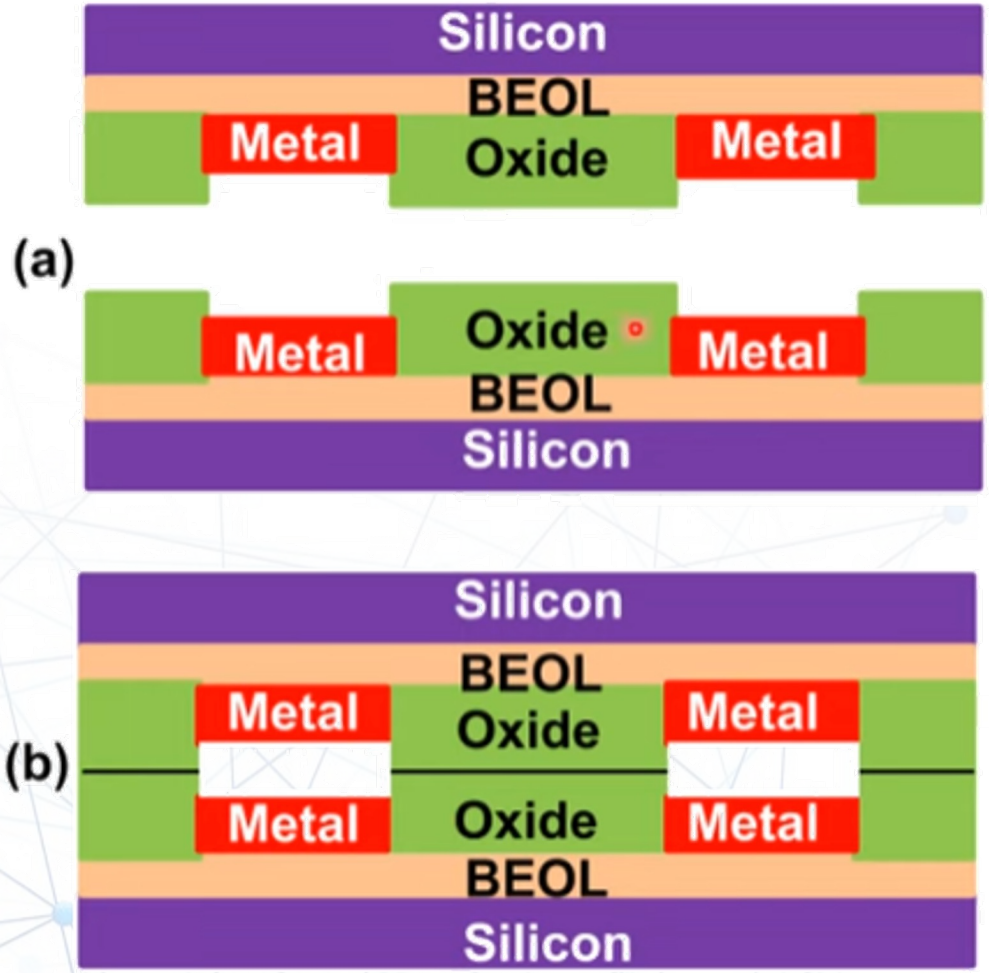
- The nano topography is extremely important for HB, the surface must be flat and smooth through CMP process.
- Small particles/surface defects can cause 10-1000s of failed connections
- Metal pads must be precisely recessed to form consistent and strong bonds.
- “Dishing” effects is used for annealing.



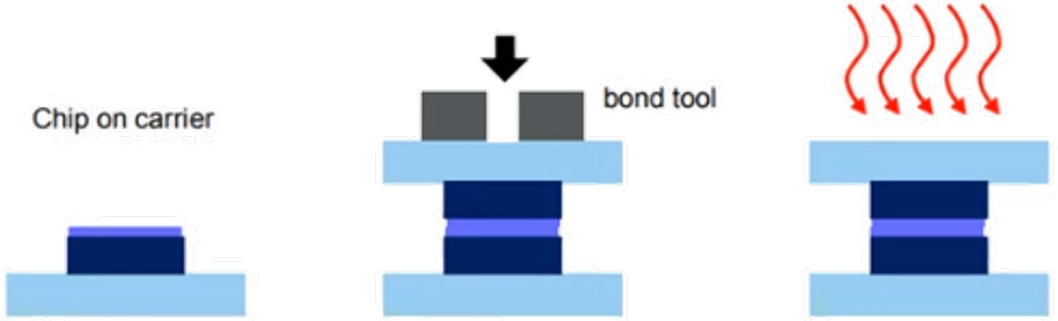


Hybrid Bonding Process

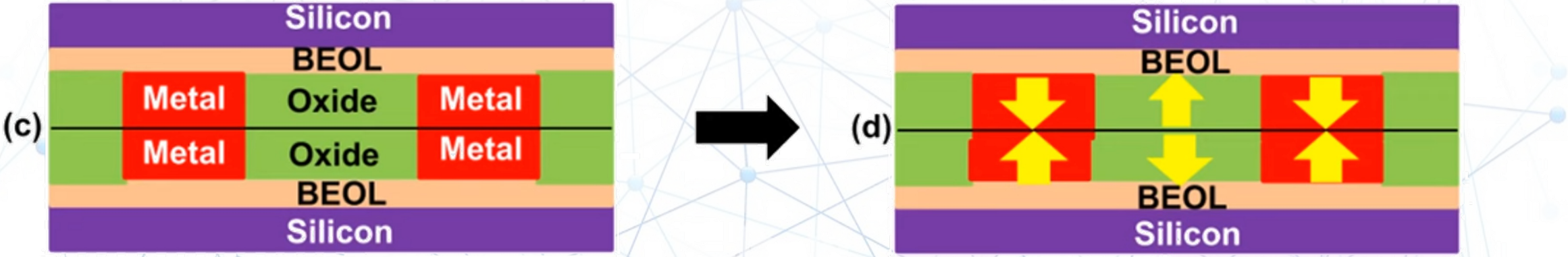
- After both surfaces are prepared, the dielectric surfaces are Plasma-activated to be hydrophilic.
- Surface activation can be evaluated with a Contact Angle Measurement.
- The two layers are brought together at room temperature and undergo Hydrophilic oxide-oxide bonding.



Hybrid Bonding Annealing Process



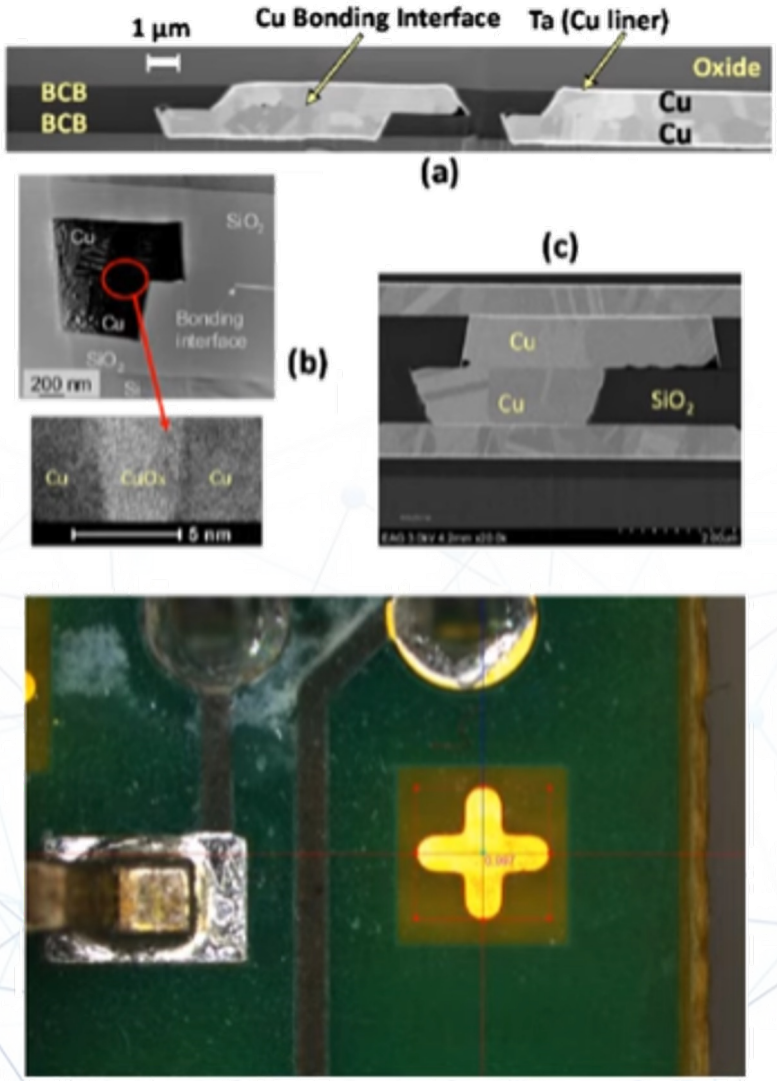
- After the oxides are bonded together, the system is annealed.
- Due to a mismatch in coefficients of thermal expansion between the oxide and metal (metal CTE > oxide CTE), the metal expands to close the dishing gap.
- Internal pressures and low heat increase the driving forces for diffusion within the metal and achieve a strong bond between surfaces. (external pressure is optional)



Placement Accuracy

- Due to the extremely small connection sizes supported by Hybrid Bonding, placement accuracy is crucial when forming the bonds.

- Size, shape, and contrast of design can be optimized to improve image recognition.
- CMP and dicing optimization, along with surface protection can improve die quality.
- Vibration, cleanliness, and thermal control along with Bond Head Parallelism can optimize the tool's function.



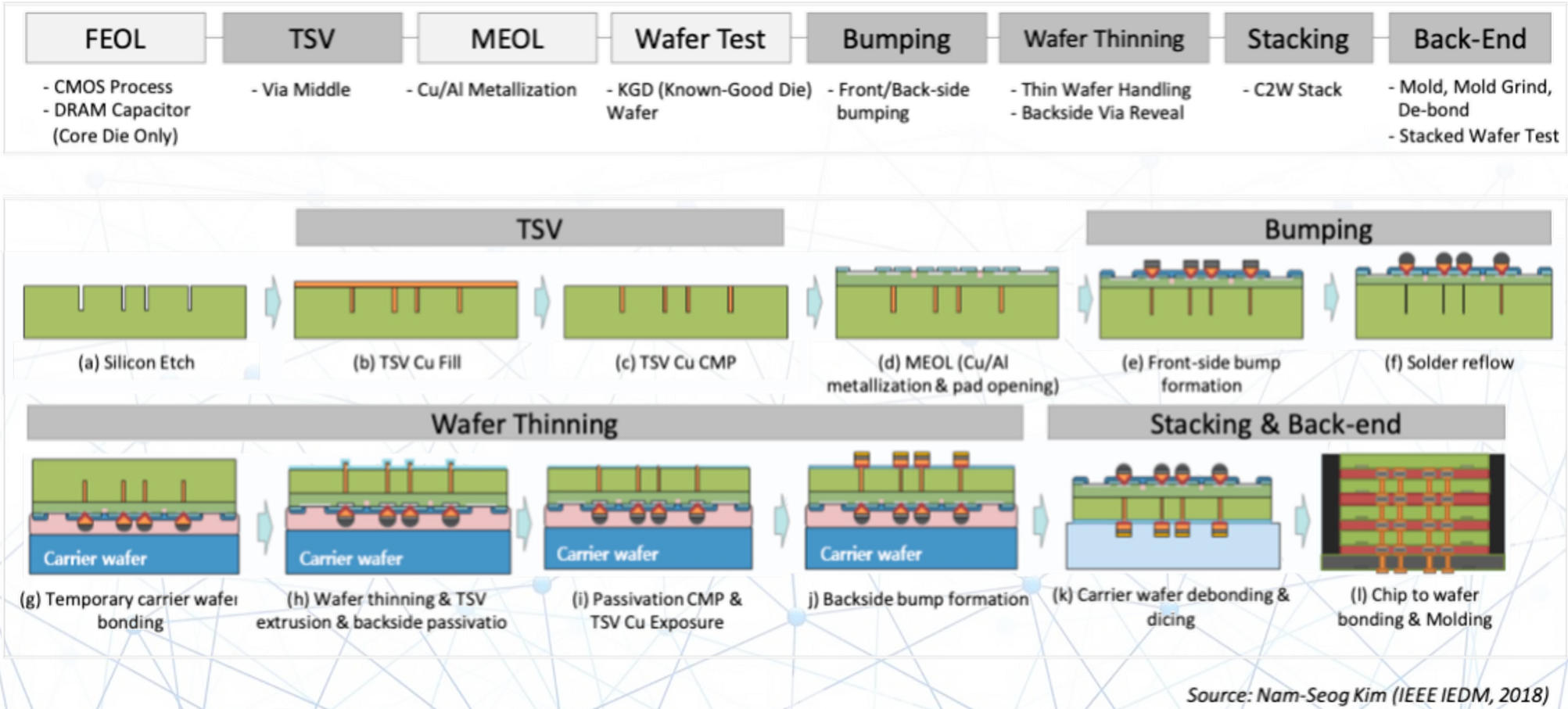
High Bandwidth Memory Roadmap

Category	Item	HBM1	HBM2	HBM2E	HBM3	HBM3E
	Time	2014	2018	2020	2022	2024
General	Die Density	2Gb	8Gb	16Gb	16Gb	24Gb
	Max Bandwidth	128 GB/s	0.3 TB/s	0.5 TB/s	0.7 TB/s	1.18 TB/s
Config.	Max Stack Height	4HI	8HI	8HI	12HI	12HI
	Capacity	1GB	8GB	16GB	24GB	36GB
	Total IO/Cube	1024	1024	1024	1024	1024

- HBM 4 is still under discussion, while many believes it will be hybrid bonding.

HBM Packaging Process

- Via Middle TSV + Double Side Micro-Bumping + Chip to Wafer Stakcing
- Known-Good-Stacking-Die Test in Wafer level

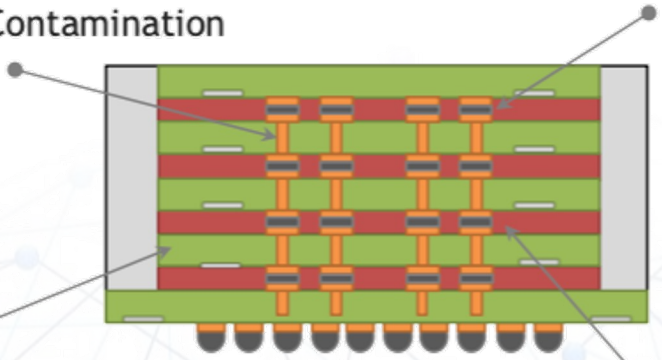


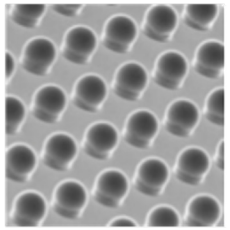
Source: Nam-Seog Kim (IEEE IEDM, 2018)

HBM Packaging Process

■ Via (TSV) Formation

- Process : Via Etch, Liner Dep, High AR Gap-Fill
- Concern : KOZ, IMD Integrity, Cu Contamination



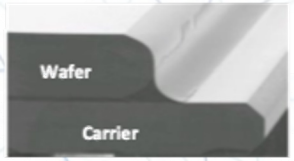


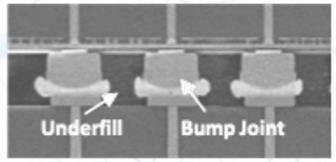
■ Bump Formation

- Process : Electroplating
- Concern : Process Uniformity, Yield
  Reliability (Mechanical/Thermal)

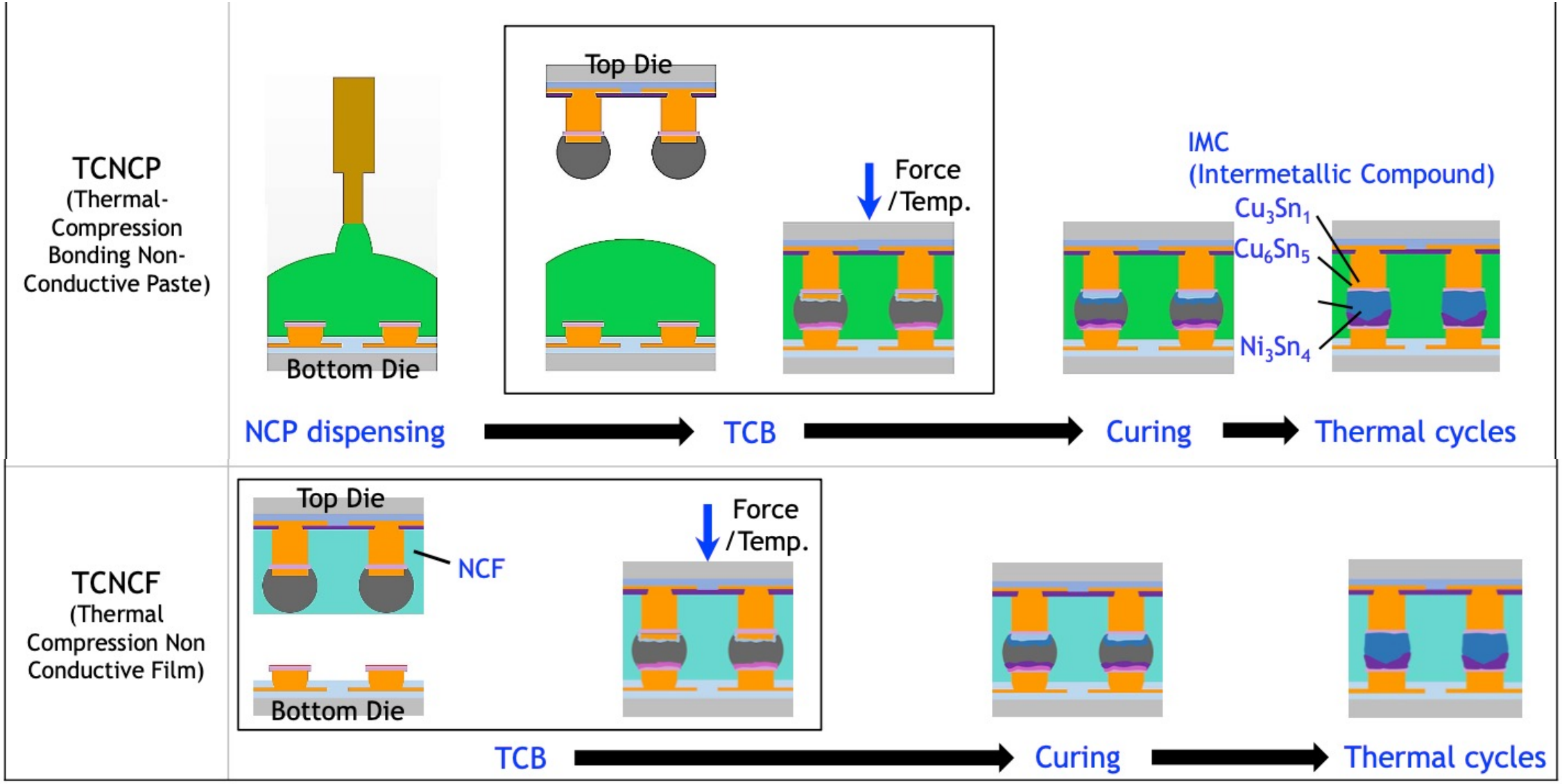
■ Wafer Thinning

- Process : Temporary wafer bonding/debonding,
  Thinning/Via Reveal
- Concern : TTV Control, Adhesive Residue, Throughput,
  Backside Passivation





■ Chip Stack/Underfill

- Process : Pre-applied Underfill (NCF), Post Gap-fill (MUF)
- Concern : Productivity, Thin Die Handling, Stress/Warpage
  Control, Reliability (Void, Adhesion, Joint Reliability)

Mass Reflow-Molded Under-Fill Process