SME737006: Advanced Packaging & Integrated Chips **(Due: 04/01/24)**

Homework Assignment #1

Instructor: Chixiao Chen, Wenning Jiang *Name:* *, FudanID:*

- This HW counts 15% of your final score, please treat it carefully.
- Please submit the electronic copy via mail: faet_english@126.com before 04/01/2024 11:59pm. Please use "Chiplet-Hmwk-1"+Your Name+Your FudanID as the mail title.
- It is encouraged to use LaTeX to edit it, the source code of the assignment is available via: https://www.overleaf.com/read/jzxjzqdrkxty#e84c79
- You can also open it by Office Word, and save it as a .doc file for easy editing. Also, you can print it out, complete it and scan it by your cellphone.
- You can answer the assignment either in Chinese or English

Problem 1: Bump/balls pitch and Density (30 points)

Compute the normalized density (assuming 16×16 array) of different types of bump/balls, and fill the blanks of the following table.

Bump/Ball Type	Pitch (um)	Normalized Density
Solder Ball	500	1x
C4 Bump	150	
Micro-Bump	40	
Hybrid Bonding Bump	5	

Problem 2: Deep-trench-capacitor process in silicon interposer (70 points)

The deep-trench-capacitor (DTC, shown in Fig.1) is a critical passive device in modern silicon interposers. It use a trench to increase the capacitor's plate area, and thus capacitance. Based on the Damascene process, please develop a DTC process on silicon interposer. A deep dive is shown in the reference paper below.

Reference: S. Y. Hou et al., "Integrated Deep Trench Capacitor in Si Interposer for CoWoS Heterogeneous Integration," *IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, 2019, pp. 19.5.1-19.5.4.

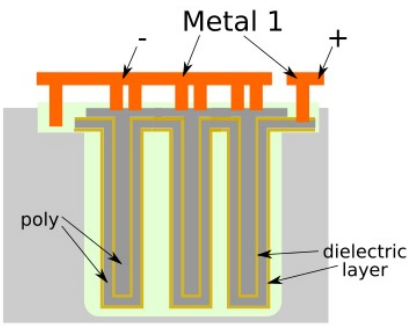

Figure 1: Cross view of deep-trench-capacitors.