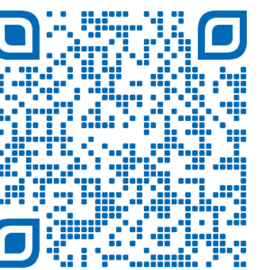
复旦大学 FUDAN UNIVERSITY

先进封装与集成芯片

Advanced Package and Integrated Chips



Lecture 2： Damascene, 2.5D Integration

Instructor: Chixiao Chen, Ph. D

Schedule

- From 2.26 to 6.10
  - 4 weeks for Advanced Packaging
  - 4 weeks for die-to-die circuit design
  - 3 weeks for integrated chips system
- Project and Presentation: May 27/Jun 3 & 10
  - 5.27 is 校庆日， to be determined (TBD)
  - 6.10 is 端午节，放假
- CICC Week (April 21-24)
- ISCAS Week (May 19-22)
- 清明节、劳动节 do not affect us so far.

第二学期　　　2024年2月18日至2024年6月29日

周次	日	一	二	三	四	五	六
0	2/18	19	20	21	22	23	24
1	25	26	27	28	29	3/1	2
2	3	4	5	6	7	8	9
3	10	11	12	13	14	15	16
4	17	18	19	20	21	22	23
5	24	25	26	27	28	29	30
6	31	4/1	2	3	4	5	6
7	7	8	9	10	11	12	13
8	14	15	16	17	18	19	20
9	21	22	23	24	25	26	27
10	28	29	30	5/1	2	3	4
11	5	6	7	8	9	10	11
12	12	13	14	15	16	17	18
13	19	20	21	22	23	24	25
14	26	27	28	29	30	31	6/1
15	2	3	4	5	6	7	8
16	9	10	11	12	13	14	15
17	16	17	18	19	20	21	22
18	23	24	25	26	27	28	29

备　注

9. 本科生线上申请补考，2月21日至25日补考，2月25日注册，2月26日上课。
10. 研究生线上申请补考，2月21日至25日补考，2月23日注册，2月26日上课。
11. 妇女节、清明节、劳动节、青年节及端午节放假以学校办通知为准。
12. 5月17日、18日第62届校田径运动会暨第5届教工趣味运动会，5月17日停课一天。
13. 5月27日建校119周年，开展校庆学术活动等。
14. 2024届本科生、研究生毕业典礼于第17周举行。
15. 通识教育课程考试安排在第16周，第17、18周为停课考试周。
16. 第二学期于2024年6月29日结束，共计18教学周（包括考试）。
17. 2024年6月30日起开展各类本科生暑期教学活动，研究生FIST课程、暑期学校等。
18. 研究生寒假、暑假时间由院系和导师根据培养计划妥善安排。
19. 教职工原则上每学期提前一周上班，延后一周开始寒暑假轮休。具体时间安排由学校办另行通知。

Overview

- Review of Integrated Chips Structure
- Damascene process and its application in Advanced Package
- 2.5D (2.xD) Integration technologies
  - Silicon TSV interposer
  - Fan Out and RDL
  - Silicon bridge

A Deep Dive on SOTA AI Chips

Back Side Metal

DRAM Memory

AI Logic Die

DRAM Memory

Memory Controller Die

Memory Controller Die

Silicon Interposer

Advanced Substrate

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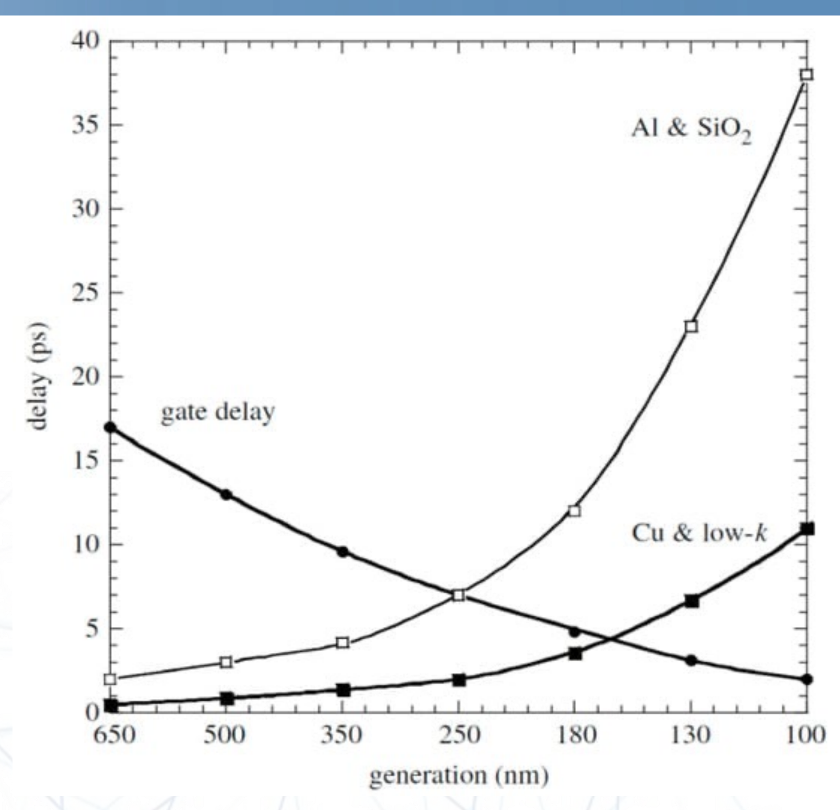
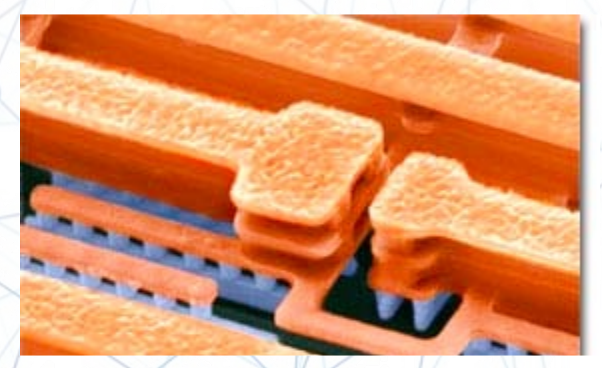
Why copper (Cu) interconnect ?

- Advantage of Cu interconnect
  - better conductivity (37%)
  - much less susceptibility to electromigration (10x)
  - enhanced heat dissipation (60%)

- Why do not use Cu in CMOS technology initially?
  - Diffuse Silicon/SiO_2 (i.e. poisonous for devices)
  - Difficult (even impossible) to etch by plasma
  - Quickly oxidizes in air





Key idea of Damascene Process

- IBM introduces Damascene Process, forming Cu interconnect, in 1990
- Why called it Damascene?
  - To make intricately patterned, highly polished steel that was used for swords and knives, metal-smiths in Damascus developed a specific technology.
  - Now, Damascus is the capital of modern Syria.

- Key idea of Damascene Process
  - Replace the copper etching with Chemical Mechanical Planarization
  - Insert a special barrier, typciall Ta, TaN, TiN, TiW, to stop copper diffusion

Single Damascene Process

1. Dielectric (SiO_2/SiN) Deposition
2. Photolithography and Dielectric Etching, leaving trenches/vias
3. Barrier layer (TiN) deposition
4. Copper deposition by electroplating or chemical vapor deposition
   - ➢ Two step: thin seed layer + thick layer
5. Chemical-Mechanical Polishing (CMP), remove the excess

Note: TiN is conductor. Damascene is additive.

Dielectric

Etch and Deposit Barrier Layer

Ta/TaN liner

Copper must be encapsulated to prevent out-diffusion

Deposit Seed Layer

Copper Seed Layer

Electro plating

Ta/TaN liner

Wafer Surface

p-Well n-Well p-Well n-Well

CMP

Copper connections between tungsten plugs

p-Well n-Well p-Well n-Well

Fig. 2: Single Damascene Process Steps [1]

Dual Damascene Process

➢ Motivation: making the inter-layer vias without separate via process.

1. Two layer Dielectric Deposition
2. Trench etching (upper layer) using lithography and plasma etching
3. Via etching (lower oxide layer)
4. Barrier layer (TiN) deposition
5. Two step copper deposition
6. Chemical-Mechanical Polishing (CMP), remove the excess copper

Resist
Dielectric
Etch Stop
Si Wafer
TiN
Copper Seed
Copper Fill

Fig. 4: Trench First then Trench [4]

The Damascene Process in TSV fabrication

- A similar process is applied for TSV application, which has approximately 10 μm opening in diameter and about 105 μm depth, which give an aspect ratio of 10.5.

Si substrate

SiO_2

SiO_2 by thermal oxidation or PECVD

Photoresist

Photoresist

Mask, Litho/ Patterning

SiO_2 etch

TSV

DRIE

Strip resist

SiO_2

Ti/Cu or Ta/Cu

PECVD or SACVD SiO_2, PVD barrier layer (Ti or Ta) and seed layer (Cu)

Cu

Cu Plating. Then anneal at 400°C for 30m

SiO_2

Cu TSV

Ti/Cu or Ta/Cu

CMP the overburden Cu, Cu seed layer, and barrier layer

100μm

TSV

0.40μm

0.44μm

10.1μm

0.83μm

8.67μm

Silicon Interposer Fabrication Process

- ➢ TSV and redistribution layer (RDL) use Dual Damascene Process
- ➢ Under bump Metallization (UBM) use nickel to serve as barrier
- ➢ The interposers are thinning to 100um to assure TSV-C4 connection

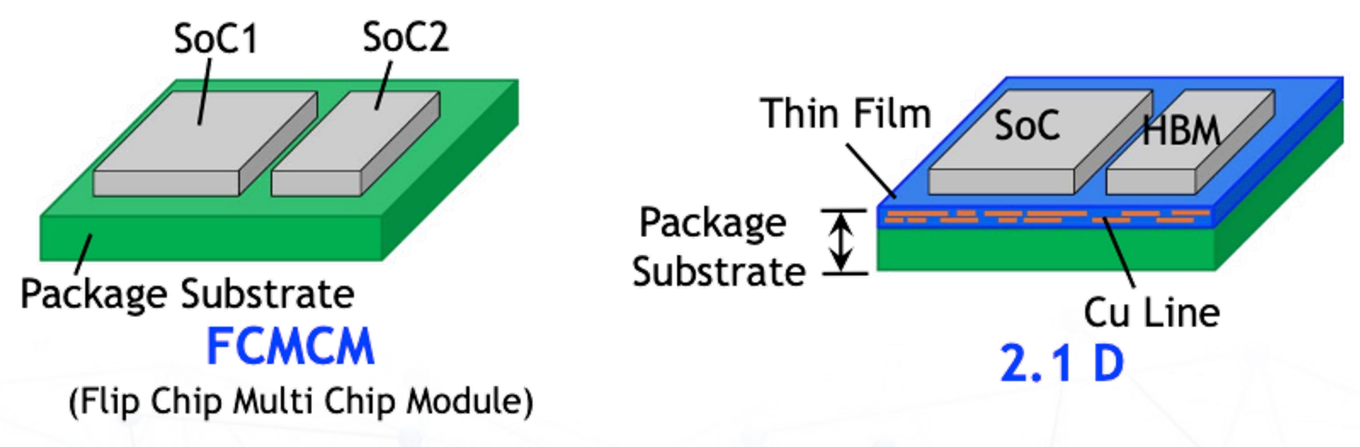
Underfill
UBM
Cu Pillar
Chip 1
Chip 2
Solder
RDLs (Redistribution layers)
RDLs for lateral communications
Underfill
TSV
Si Interposer
UBM
Solder Bumps
Package Substrate
Build-up Layers
Solder Balls

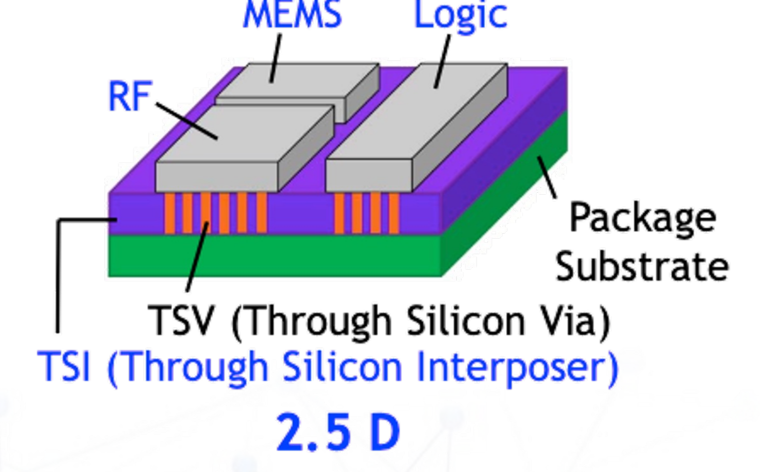
Solder bump
UBM
RDL
Metal pad
Wafer
RDL
Metal pads
Redistributed bumps

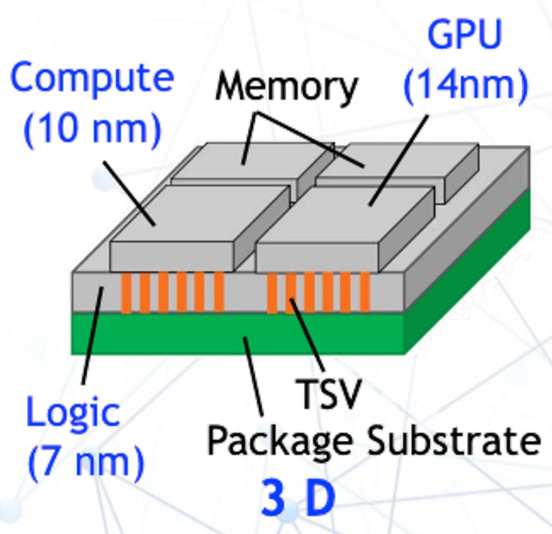
TSV (Cu)
SiO_2
SiO_2
Si
Ta/Cu or Ti/Cu
SiO_2
TSV
SiO_2 by PECVD
TSV
Photoresist
TSV
Mask aligner or Stepper, litho
TSV
RIE of SiO_2

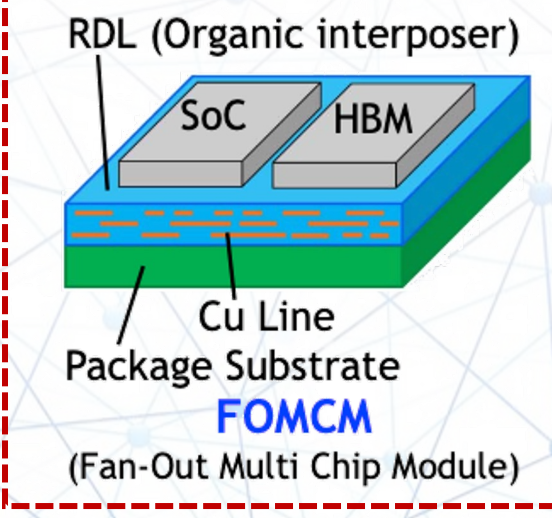
TSV
Mask aligner or Stepper, litho
TSV
RIE of SiO_2
TSV
Strip resist
TSV
V01
Sputter Ti/Cu and plate Cu
RDL1
TSV
V01
CMP Cu and Ti/Cu
DL2
RDL2
V12
DL1
RDL1
V01
TSV
DL12
DL01

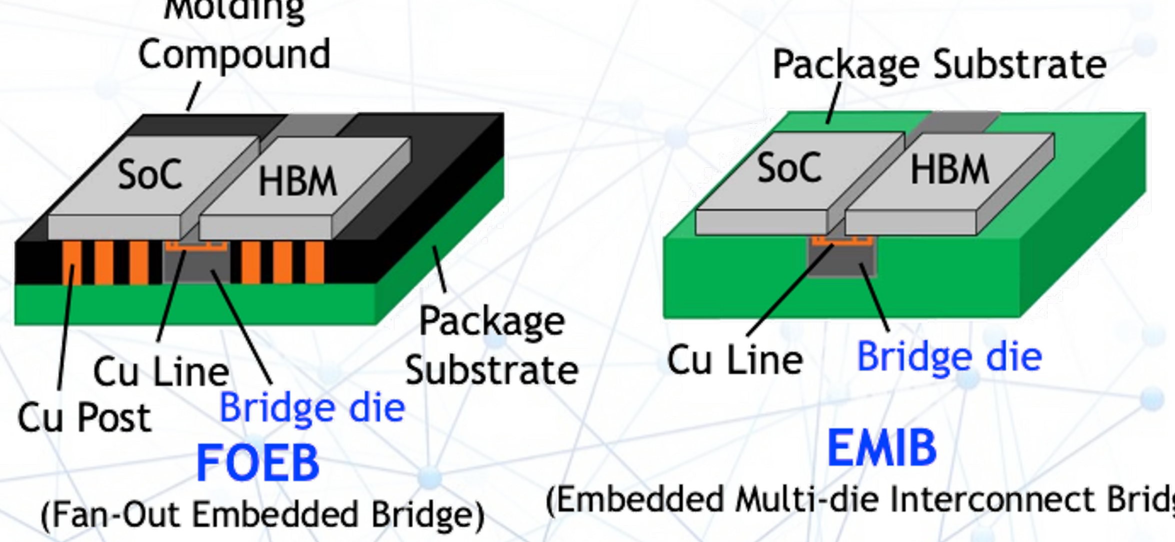
Categories of 2D-2.5D Chiplet Integration











Source: C.K Chung VLSI 2020

Packaging Flow for Silicon Interposer

- Die-last Chip-on-Wafer (CoW) flow
- Interposer can be tested before CoW process
- Thin wafer to CoW
- Need 2x glass carrier
- Question: Which company complete the Front/Middle/Back end process?
  - OSAT: Outsource Semiconductor Assembly and Test
  - Semiconductor fab

Passivation
Si Substrate
TSV
UBM
RDL/Pass.

Carrier #1
Interposer
Temporary Bonding

Carrier #1
Backgrinding

Carrier #1
Si Etching, Pass., and Cu Revealing

Carrier #1
UBM

Carrier #1
C4 Wafer Bumping

Carrier #1
Carrier #2
Temporary Bonding Carrier #2

Carrier #2
De-bonding Carrier #1

Carrier #2
Chip-on-Wafer. Underfill

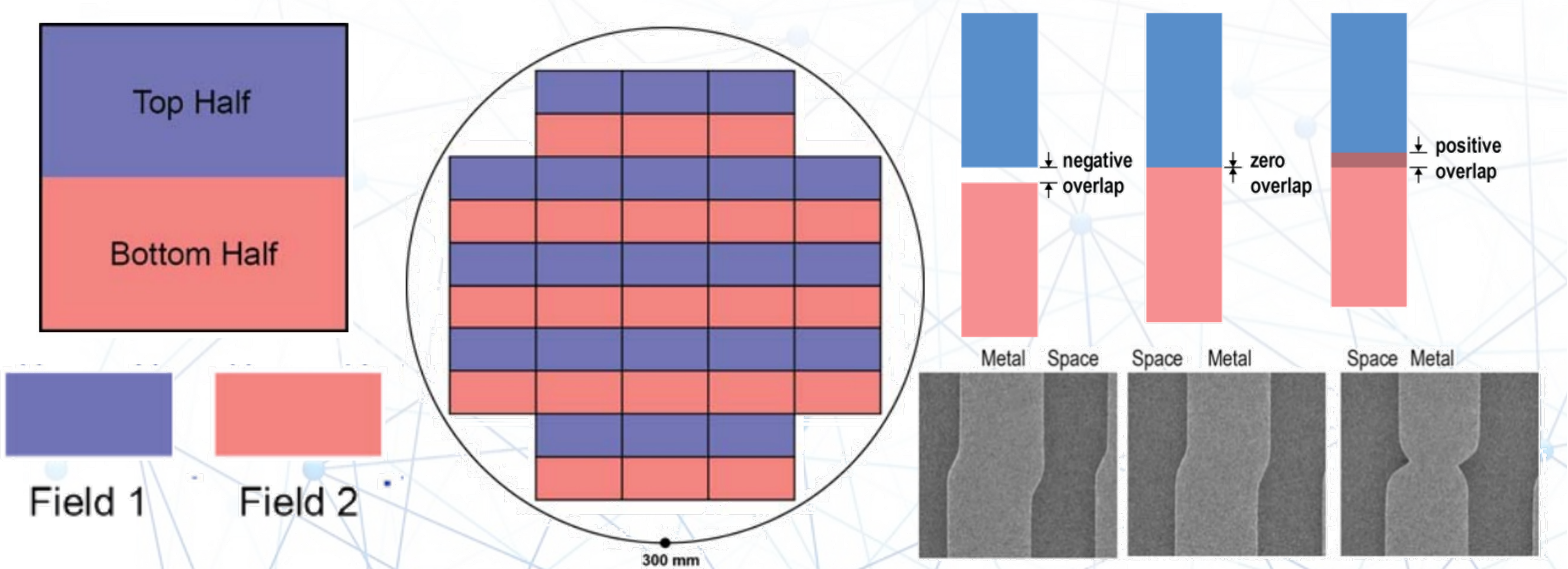
De-bonding Carrier #2 and dicing

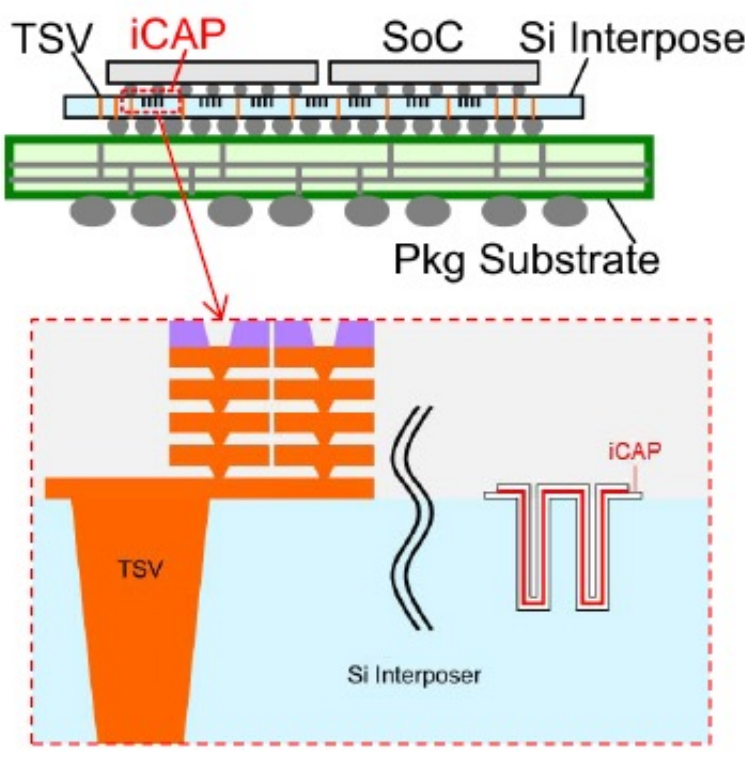
Chip
TSV
Interposer
Package Substrate
Assemble the TSV module on package substrate, then test. Underfill

Not-to-scale

Adanced Silicon Interposer Technology

- To fabricate an interposer whose area is larger than reticle size, splitting and stitching is needed. Lithography stepper has less resolution at stitching boundaries.
- To enhance the power integrity, deep trench capacity (DTC) is required, like DRAM. DTC is embedded in silicon interposer with high-k dielectronic.





Roadmap of CoWoS-S Technology

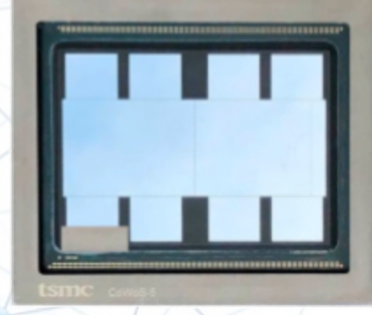
- TSMC has developed 5+ generation of Silicon interposer (CoWoS-S) technology
- The main progress is the area of the interposer
- Challenges include warpage and cost.

Top die
Solder bridging
Si interposer
Non wet
(a)
Laminate

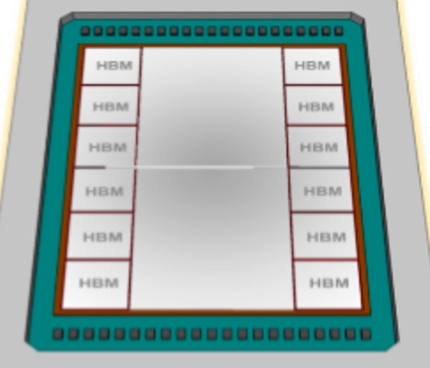
2011
1.0X

2016
1.5X, 4 HBM

2019
2X, 6 HBM



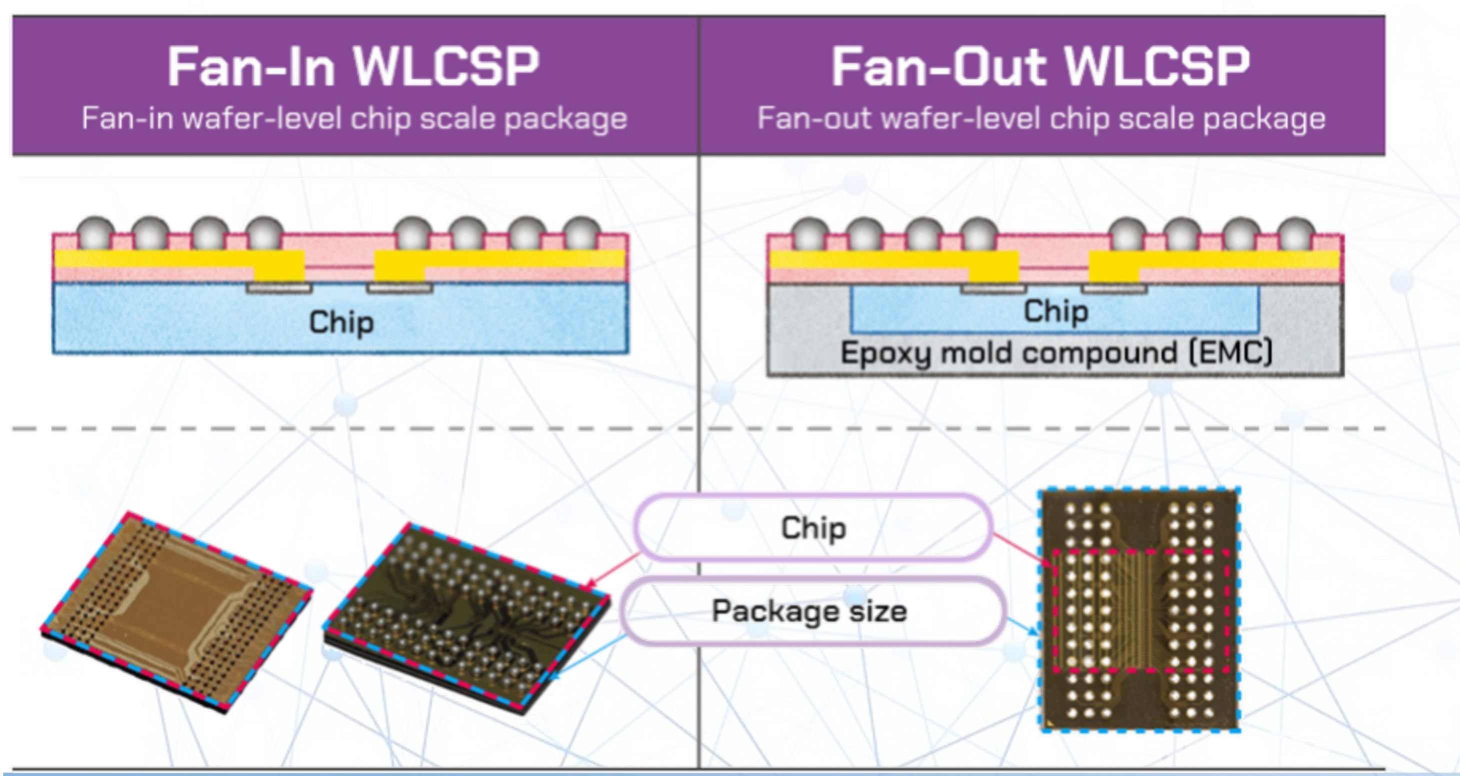
2021
3x, 8 HBM

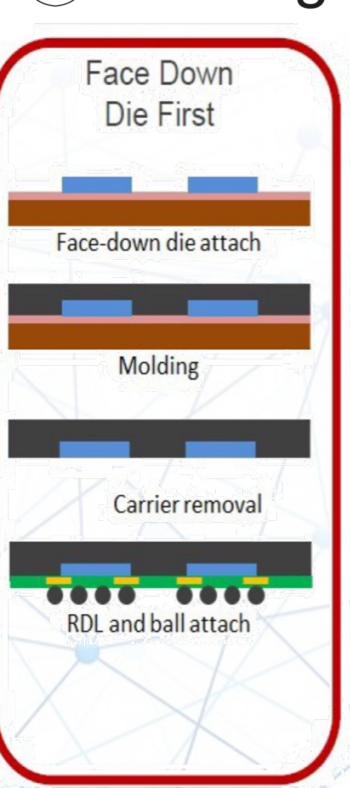


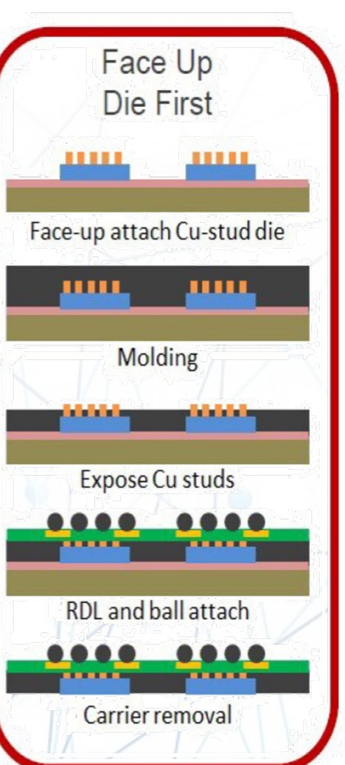
2023
4x, 12 HBM

Fan-Out Wafer Level Packaging Technology

- Fan-out wafer level packaging embeds multiple chips directly onto a thin carrier wafer (not in silicon). "OUT" means that paces are allocated around each chip.
- Chip-first with die face down: ① place on a carrier ② Epoxy Molding ③ RDL
  Chip-first with die face up: ① Cu stud and Die attach ② Molding ③ grindling ④ RDL







Organic Interposer Using Chip Last

- Issues of Chip first technology: die drift due to molding process. Limited routing metal L/S (10μm for Face down, 5μm for face up)
- Chip-last / RDL-first is developed to reduce the minimum L/S to 2μm.

1. Temporary carrier coated with release layer
2. Seed layer deposition
3. Photoresist coat, patterning and electroplating
4. Photoresist strip, metal etch
5. Coat, pattern and cure polyimide layer
6. Repeat steps 2 through 5 for creating multiple RDLs
7. Ball attach, die bonding, epoxy molding, mold grinding
8. Release carrier, clean release material from device wafer

① Release layer coating
② Seed layer deposition
③ Metal Patterning
④ Dielectric Layer
⑤ Pad/Lead
⑥ C2W (RDL Interposer)
⑦ Molding and Underfill
⑧ Remove the carrier

" Organic RDL interposer "

Packaging Flow Comparison for Fan Out

Method	Chip First		Chip last
	Face up	Face down	Face down
Process flow	(a) Chip DB (b) Reconstitution (c) RDL (d) Backend (C4 + sawing)	(a) Reconstitution (b) RDL (c) Backend (C4 + sawing)	(a1) Chip (a2) RDL (b) Flip Chip assembly (c) Backend (C4 + sawing)
Advantages	• Low die shift • Good RDL routability	• Low cost • Good RDL routability	• RDL No Die lost • Better RDL routability • Lower thermal budget • Higher reticle sizes • Faster cycle time • Better reliability
Dis-advantages	• Die lost concern • Higher thermal budget • higher cost (2 glass carriers)	• Die lost concern • Higher thermal budget • Die shift • Reticle size Limitation	• Higher cost (2 glass carriers) • Additional Underfill processes

Fan-Out for Ultra High Performance Computing

- Full wafer integration (System-on-wafer) is an emerging technology for ultra-high performance computing and high bandwidth die-to-die communication.
- Leveraging Fan-Out technology is a SoW solution with Known-Good-Dies. It also allows heterogeneous integration of compute/IO/… chiplets and integrated power.

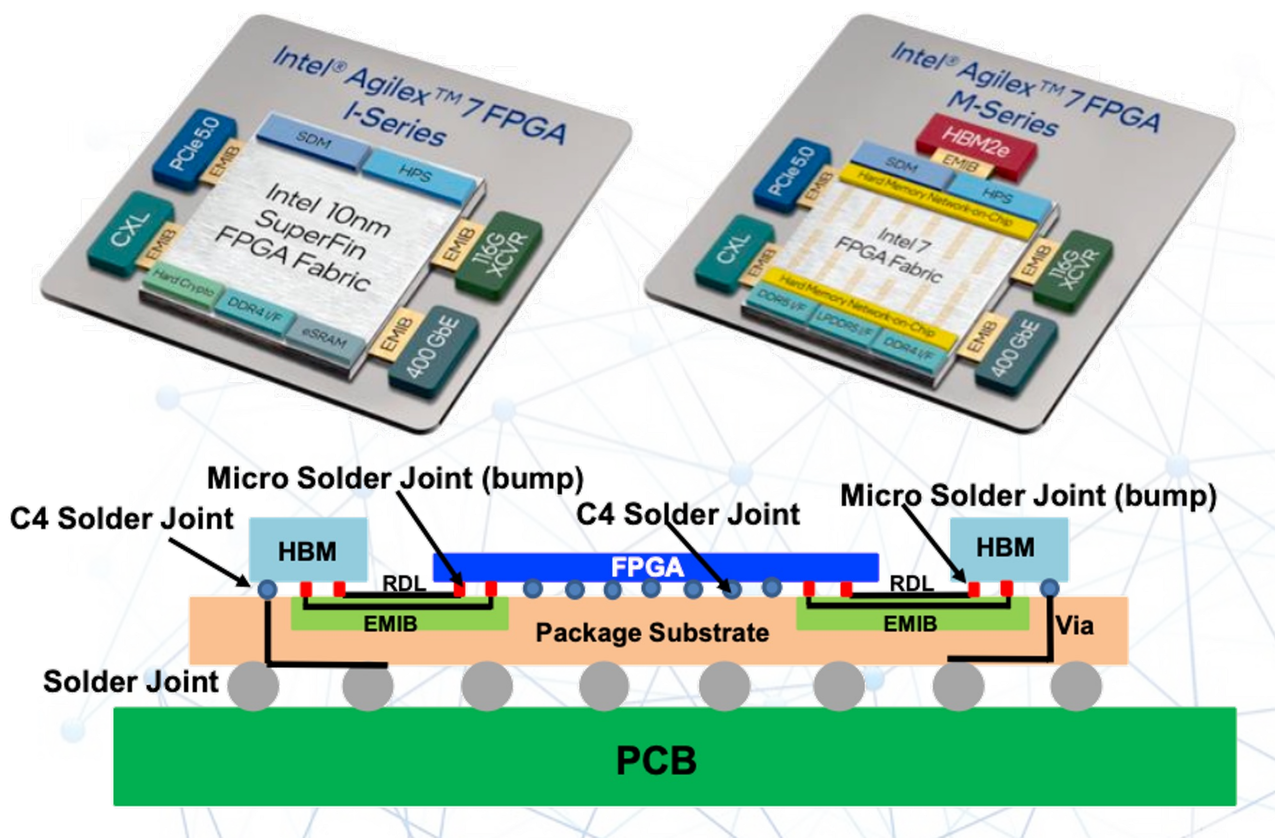
Tesla Dojo supercomputer is the first industry full-wafer heterogeneous integration technolgy with good process control and high quality RDL.

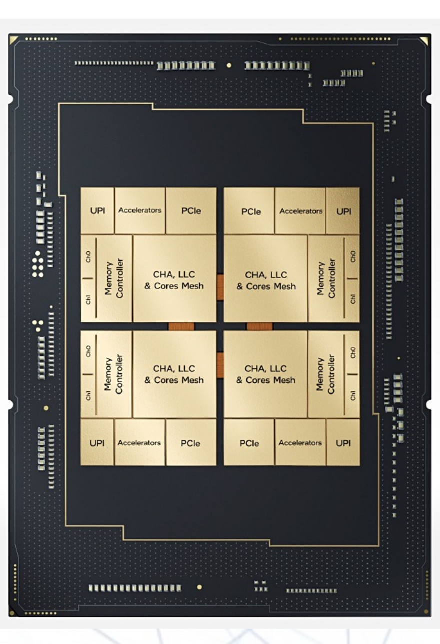
Mimic power module
Connector
InFO wafer
Mimic thermal module (Cold Plate)

Power Module
Connector
Chip 1
Chip 2
Chip 3
Thermal Module

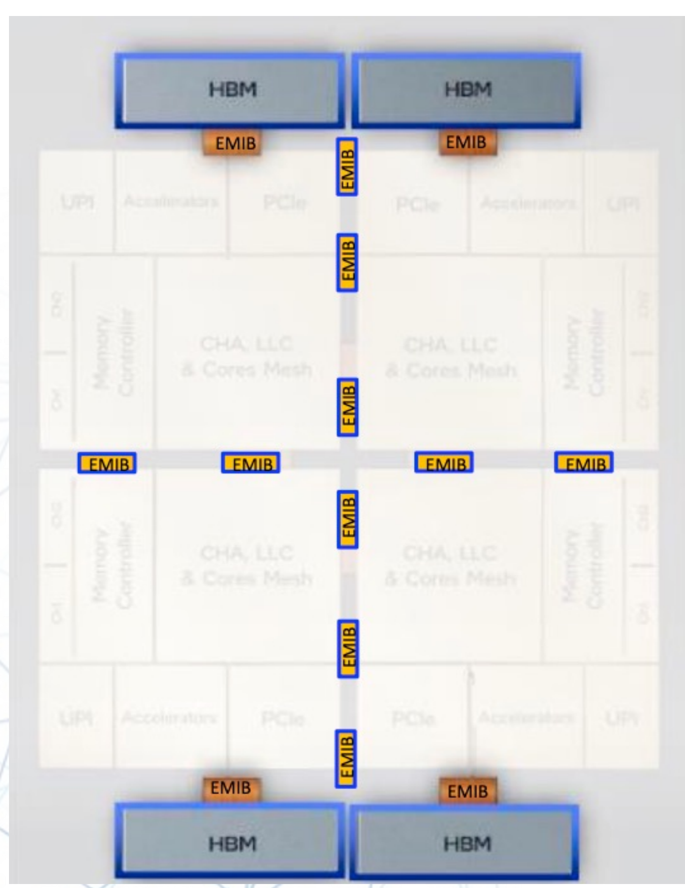
What is Silicon Bridges and Why?

- Large area silicon interposer with TSV has extremely high.
- High density interconnect only occurs in local and small area.





第四代英特尔 至强
Xeon 可扩展处理器



Bridges Embedded in Substrate Process

Die2
Die1
Die3

FCBGA Substrate with bridge Silicon for local interconnects between multiple die

Embedded Bridge

Fine Pitch Vias and Flip Chip Interconnects

DIE 1
DIE 2
Silicon Die
55 um pitch bumps
130 um pitch bumps
Silicon Bridge

Source: Prismark (Intel EMIB 2020)

EMIB
Via

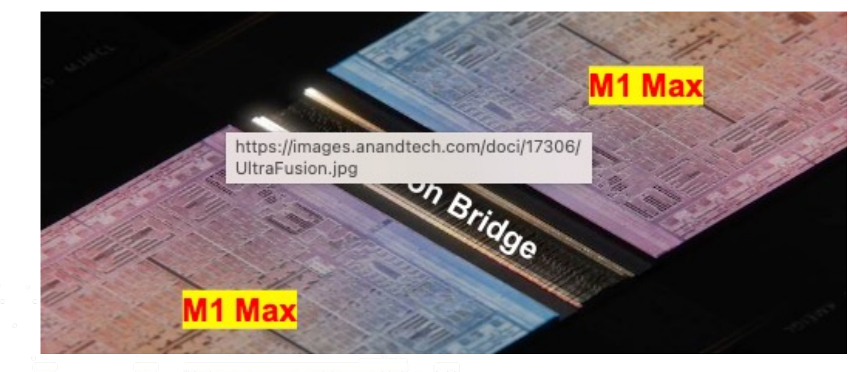
Cavity Formation → Bridge Placement → Dielectric Lamination → (Fine + Coarse) Via Drilling → Via Plating Drilling

Process flow

Source: Ravi Mahajan, IEEE ECTC 2016, 557

Bridges Embedded in Epoxy Molding Compound

- FanOut technology use Epoxy molding compound (EMC) with RDLs, achieving 2μm line width
- Apple UltraFusion technology: 2xM1-Max = M1 Ultra



heat spreader
thermal paste
encapsulant
processor 1
processor 2
bridge interconnect
top build-up
solder ball
Si bridge
core
base PWB
via
bottom build-up
solder ball
1 mm
RDLs
C4 bump

M1 Max
M1 Max

M1 Max
RDL 1 (Cu)
RDL 2 (Cu)
Cu bump
CuSn solder
Si bridge
25 μm
EHT = 5.00 kV
Width = 151.1 μm
20 μm
APL1W06_402481_DS

InFO_LSI
Chip 1
Chip 2
LSI

Originally called InFo-LSI
Now, CoWoS-L by TSMC

Fan-Out Embedded Bridge Process

- Cu pad/post are first built, and followed by molding and grinding to reveal post. Then, RDL fabrication and top die bonding.

(i) Cu Post Fabrication & Bridge die attach

(ii) Organic interposer fabrication

(iii) RDL fabrication

(iv) Logic and memory die assembly

(v) C4 bump fabrication

(vi) Flip Chip assembly

The good scalability of Fan-Out Bridge

➢ Molding compound can achieve large area much easier than Si-interposer.

Active die

Bridge die

A-A Cross-section

Active die

Bridge die

A

A

(a) 18 Dies

(b) 7 Dies

(c) 17 Dies

(d) 9 Dies

(e) 5 Dies

(f) 8 Dies

(g) 5 Dies

(h) 3 Dies

Comparison table to choose the technology I

Platform (Ref. Flip Chip MCM)		2.5 D	FOMCM	
			Die first	Die last
Supply Chain	Cost	Highest	high	Higher
	Cycle time	1.5 X	2 X	1.5 X
	Yield (%)	> 99	> 99	> 99
Chip Module	Die QTY	2 ~ 8	2 ~ 10	2 ~ 10
	Interposer	TSI	Organic/RDL	Organic/RDL
	I/O Counts	Very high	Very high	Very high
	μJoint (size/pitch, μm)	Solder, > 25/40	Solder, > 25/40	Solder, > 25/40
	Cu Line (L/S, μm)	< 2 / 2	> 4 / 4	> 2 / 2
	Chiplets integration	> 2	2	> 2
	Design Scalable	Yes	Limited	Yes
	Warpage	Controllable	Controllable	Controllable
Package	Size	> 55*55	< 55*55	> 55*55
	Warpage	Low	High	Low
	C4 Stress	Very High	Low	Low

Comparison table to choose the technology II

Platform (Ref. Flip Chip MCM)		FOEB	EMIB
Supply Chain	*Supply Chain*	Simple	Complex
	Assembly Cycle time	High	Std Flip chip process (Exclude substrate fabrication time)
	Yield (%)	> 99	80 ~ 90% (Include substrate embedded bridge)
Chip	*Die QTY*	3 ~ 30	3 ~ 16
	Interposer	Organic/RDL	Organic Substrate
	I/O density	Very high	Std. Flip chip
	μ-Joint (pitch, μm)	25~40	-
	Cu Line (L/S, μm)	0.8/0.8 ~ 10/10 (Scalable)	> 5/5
	Chiplets integration	Excellent	Excellent
	Design Scalable	Good	Good
	Warpage	Low	Low
Package	*Size (mm^2)*	> 55*55	> 55*55
	Coplanarity	Comparable	Comparable
	C4 Stress	Low	Depend on die size