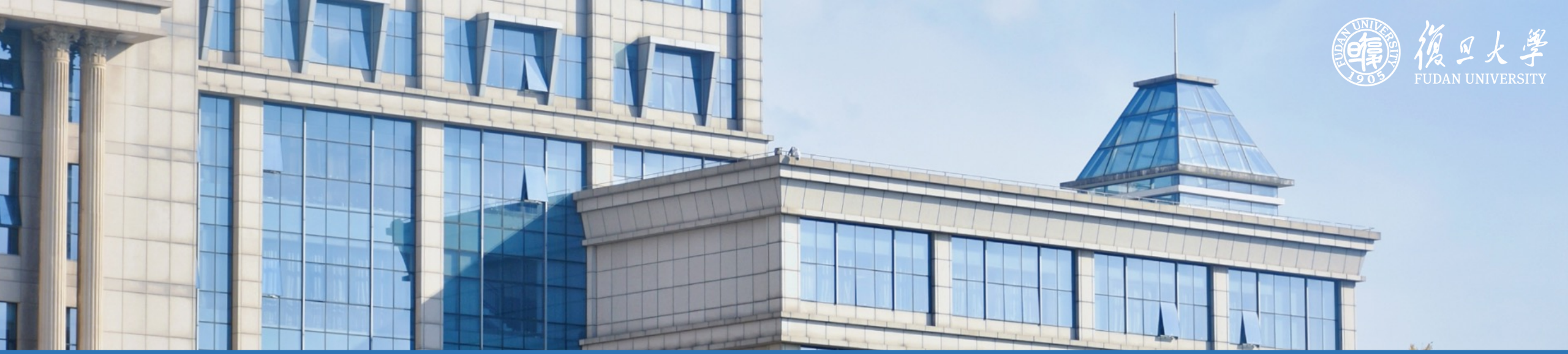


先进封装与集成芯片

Advanced Package and Integrated Chips

Lecture 1： Introduction

Instructor: Chixiao Chen, Ph. D

Overview

- Course Overview
- Difference between Conventional Packaging and Advanced Packaging
- Chiplet and Integrated Chips

Course Information

- Instructor I: Chixiao Chen
  Email: cxchen@fudan.edu.cn
- Instructor II: Wenning Jiang
  Email: wenningjiang@fudan.edu.cn

陈迟晓

江文宁

- Location: JA204, Jiangwan Campus
- Time: Monday Night 18:30 - 21:05
- Website: https://cihlab.github.io/course/chiplet.html
- WeChat Group Chat

Textbook

- English version can be downloaded if you have Fudan account via Springer website.
- Chinese version can be purchased.

- High speed D2D Circuits and Systems: https://people.engr.tamu.edu/spalermo/ecen720.html

Contents, Exam and Score

- Motivation: This course is not an packaging course, but a circuit and system design guide with advanced packaging knowledge.
- 3 parts: 1) Advanced Packaging by Chixiao Chen
  2) Inter-chip communication circuit design by Wenning Jiang
  3) Integrated Chips Architecture by Chixiao Chen
- Exams: 1) Option 1: Presentation (Related Papers form ECTC, ISSCC …)
  Option 2: Project Design (UCIe Package/PHY/Controller Design)
- Score: 20% Attendance/Quiz + 20 % Homework + 60% Presentation/Project

Schedule

- From 2.26 to 6.10
  - 4 weeks for Advanced Packaging
  - 4 weeks for die-to-die circuit design
  - 3 weeks for integrated chips system
- Project and Presentation: May 27/Jun 3 & 10
  - 5.27 is 校庆日， to be determined (TBD)
- CICC Week (April 21-24)
- ISCAS Week (May 19-22)
- 清明节、劳动节 do not affect us so far.

第二学期　　2024年2月18日至2024年6月29日

周次	日	一	二	三	四	五	六
0	2/18	19	20	21	22	23	24
1	25	26	27	28	29	3/1	2
2	3	4	5	6	7	8	9
3	10	11	12	13	14	15	16
4	17	18	19	20	21	22	23
5	24	25	26	27	28	29	30
6	31	4/1	2	3	4	5	6
7	7	8	9	10	11	12	13
8	14	15	16	17	18	19	20
9	21	22	23	24	25	26	27
10	28	29	30	5/1	2	3	4
11	5	6	7	8	9	10	11
12	12	13	14	15	16	17	18
13	19	20	21	22	23	24	25
14	26	27	28	29	30	31	6/1
15	2	3	4	5	6	7	8
16	9	10	11	12	13	14	15
17	16	17	18	19	20	21	22
18	23	24	25	26	27	28	29

备　注

9. 本科生线上申请补考，2月21日至25日补考，2月25日注册，2月26日上课。
10. 研究生线上申请补考，2月21日至25日补考，2月23日注册，2月26日上课。
11. 妇女节、清明节、劳动节、青年节及端午节放假以学校办通知为准。
12. 5月17日、18日第62届校田径运动会暨第5届教工趣味运动会，5月17日停课一天。
13. 5月27日建校119周年，开展校庆学术活动等。
14. 2024届本科生、研究生毕业典礼于第17周举行。
15. 通识教育课程考试安排在第16周，第17、18周为停课考试周。
16. 第二学期于2024年6月29日结束，共计18教学周（包括考试）。
17. 2024年6月30日起开展各类本科生暑期教学活动，研究生FIST课程、暑期学校等。
18. 研究生寒假、暑假时间由院系和导师根据培养计划妥善安排。
19. 教职工原则上每学期提前一周上班，延后一周开始寒暑假轮休。具体时间安排由学校办另行通知。

Electronic Packaging

Electrical connectivity:

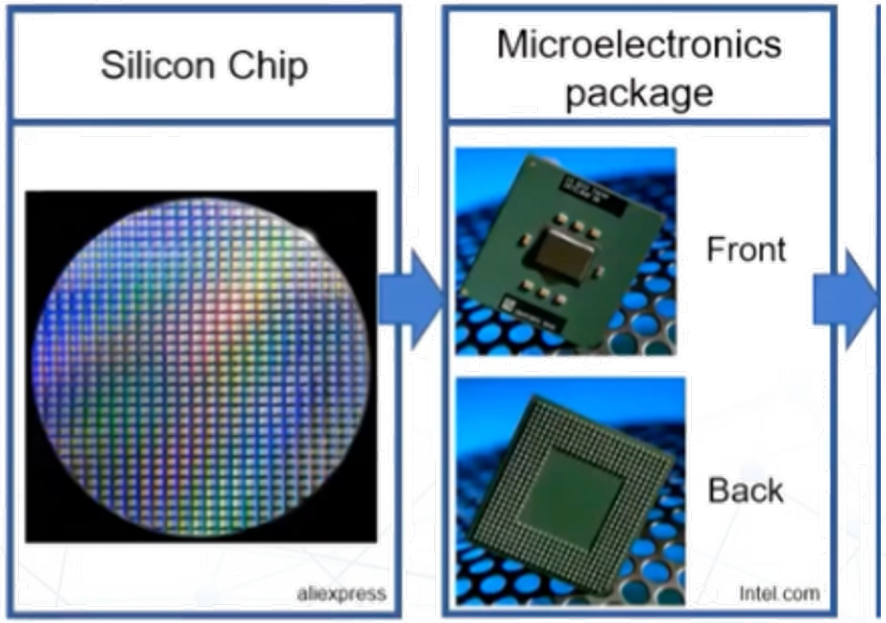
- Power distribution to all components and chip circuits.
- Connectivity between various chip circuits, devices and components.

Thermal sink:

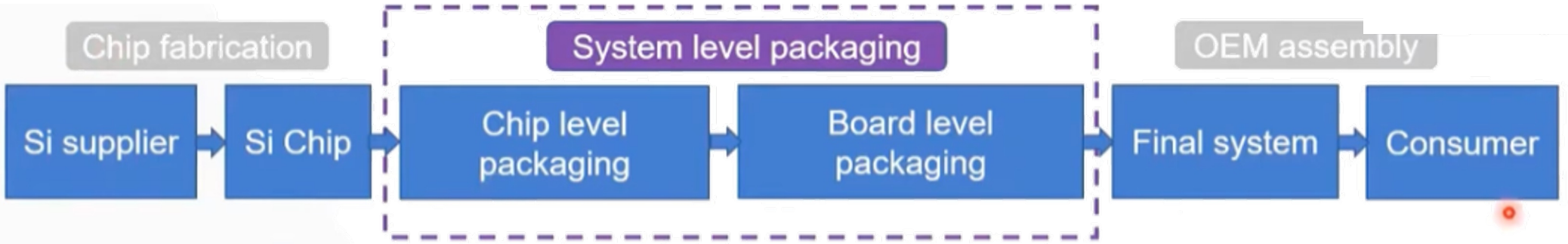
- Removal of heat generated by chip circuits during processing for continued performance.

Mechanical protection:

1. Mechanical structure and stability to allow for manufacturability.
2. Protection of devices and components from environmental exposure and damage.
3. Shielding chip circuits from external electromagnetic (EM) radiation or interference.

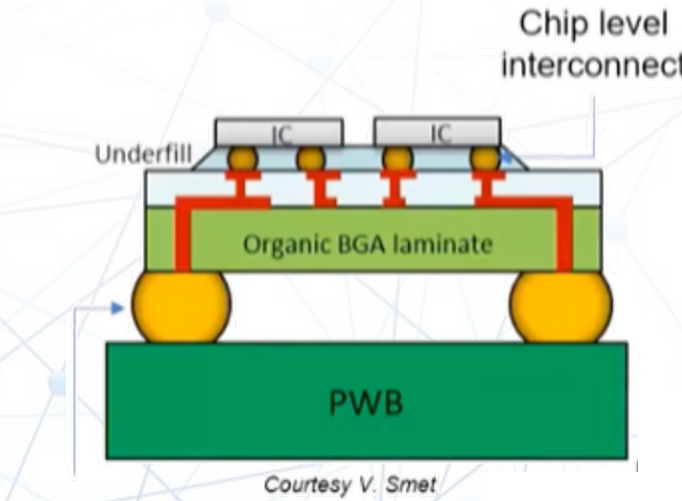


Interconnect via System Packaging



Parameter	Chip level interconnect	Board level interconnect
Level	Chip-to-package	Package-to-board
Pitch	10s of um to ~200um	Hundreds of um to ~1000 μm
Bump	Plating, jetting, dip transfer	Screen-printing, ball drop, jetting
Assembly	2D conventional, 2.5D w/ organic RDL 2.5D w/ Si interposer 3D Chip-wafer, wafer-wafer attach	Reflow, mount
Materials	Solder, flux Underfill, mold Thermal interface materials	Solder, flux Underfill (for limited applications)
Interconnection rework	Limited	Most applications
Cost	Low-moderate (depending on assembly architecture)	As low as possible

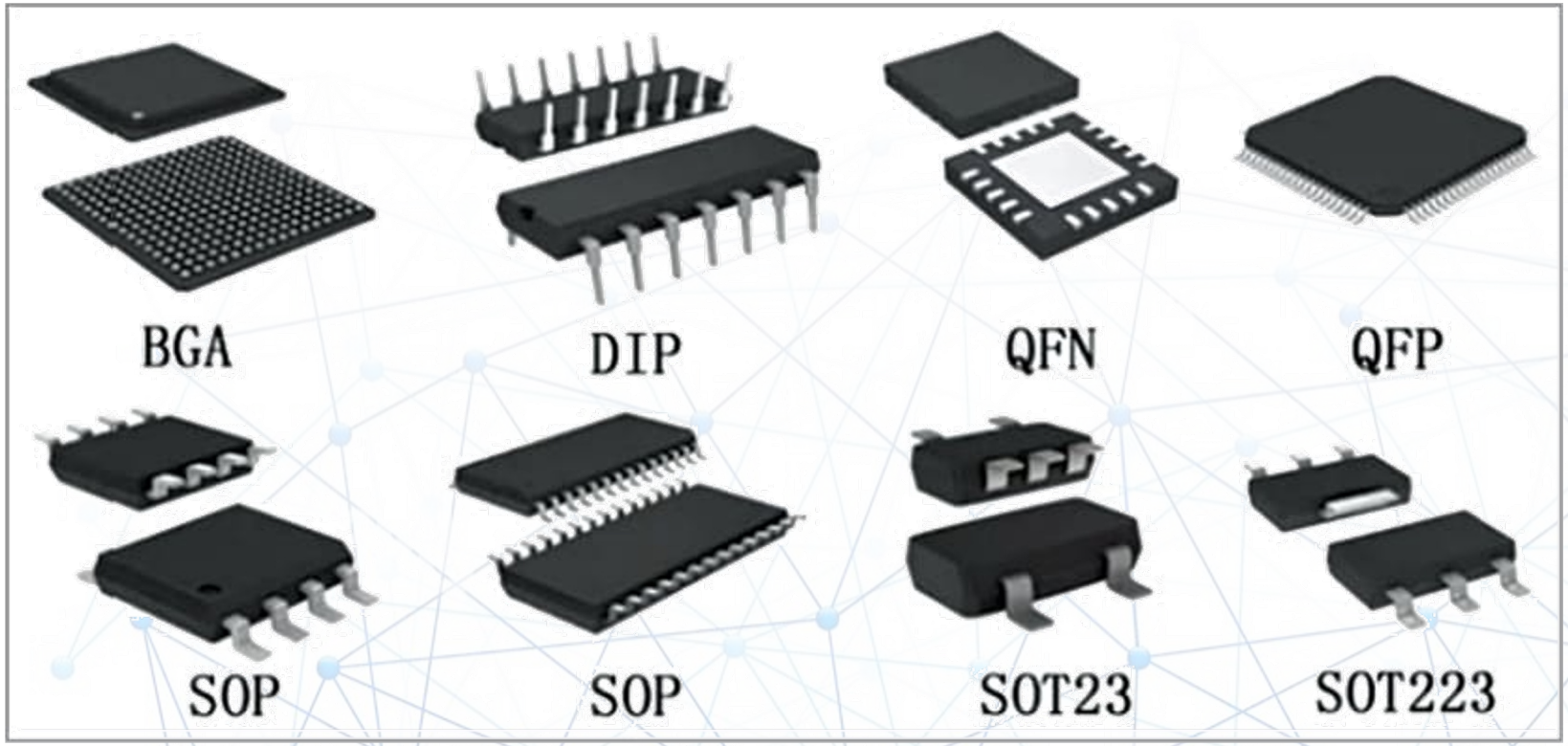
Conventional Package Architecture

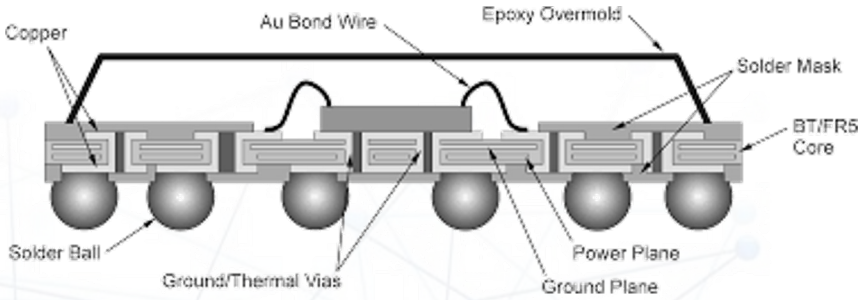


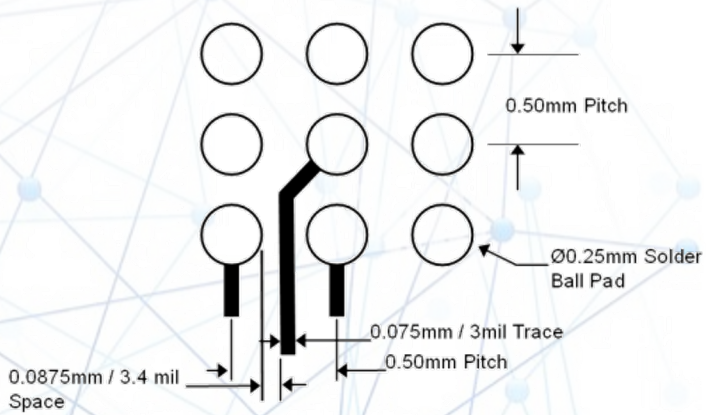
Courtesy 3DPRC, GATech

Conventional IC Package Types

- There is a number of package types, among which BGA (ball grid array) has the most interconnect.

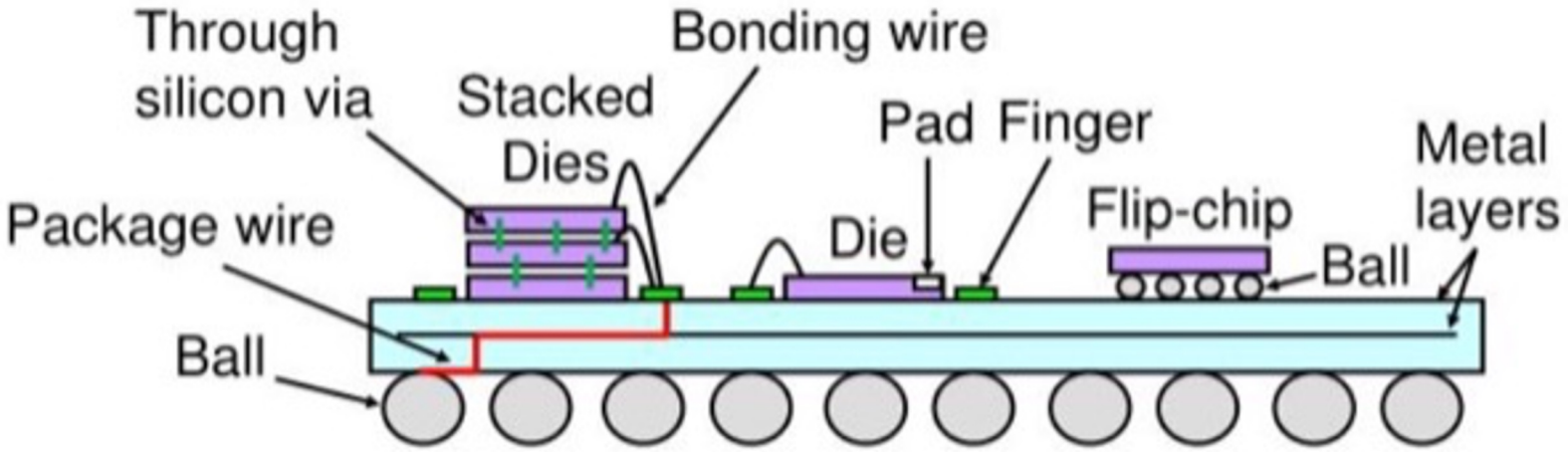


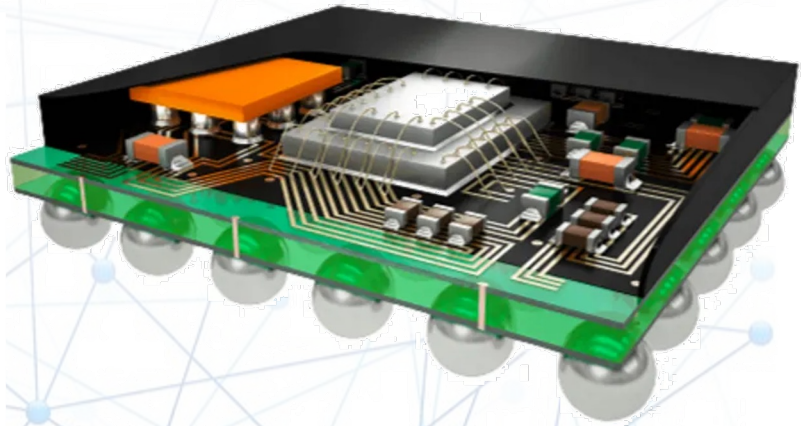




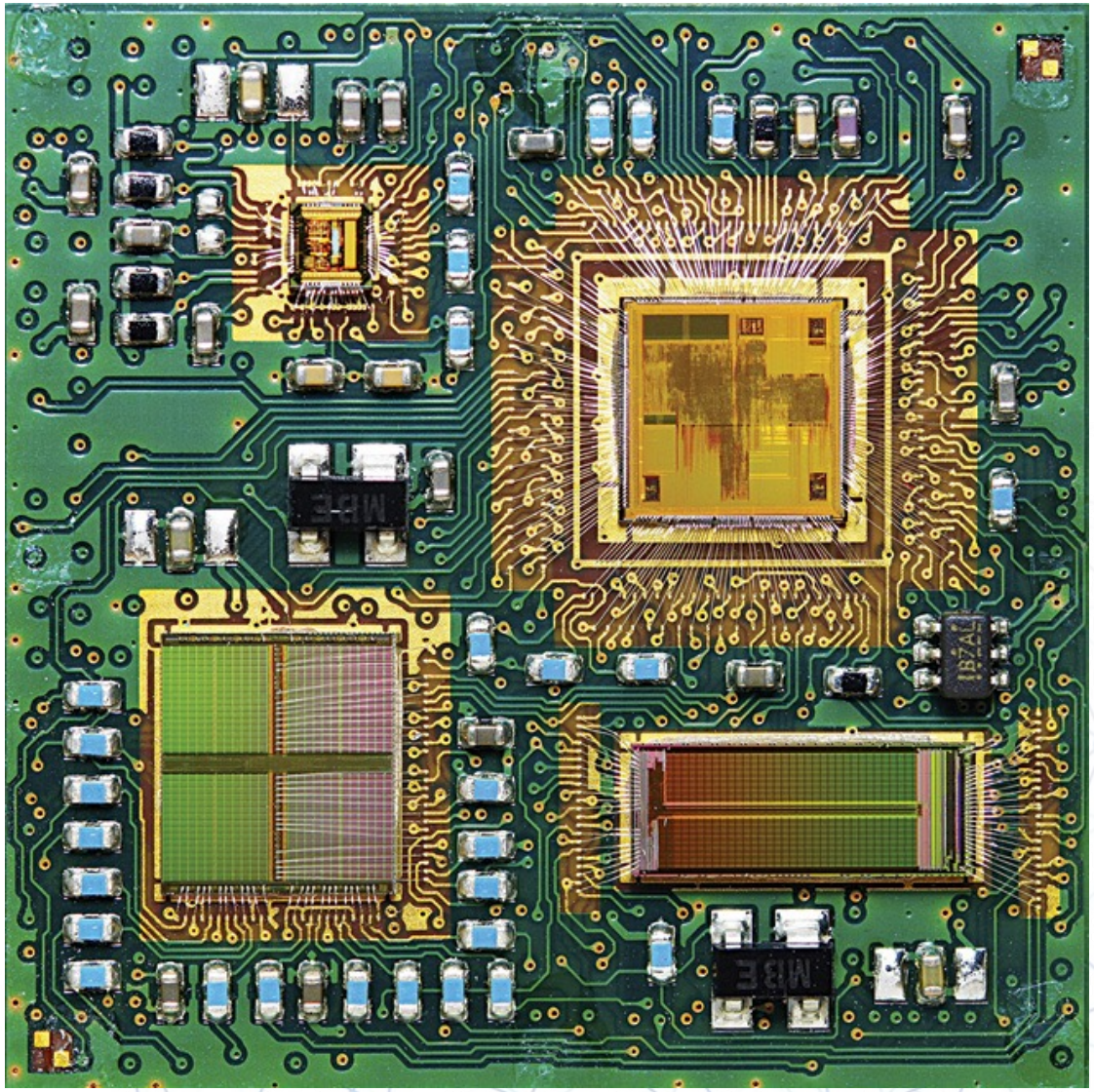
System-in-Package

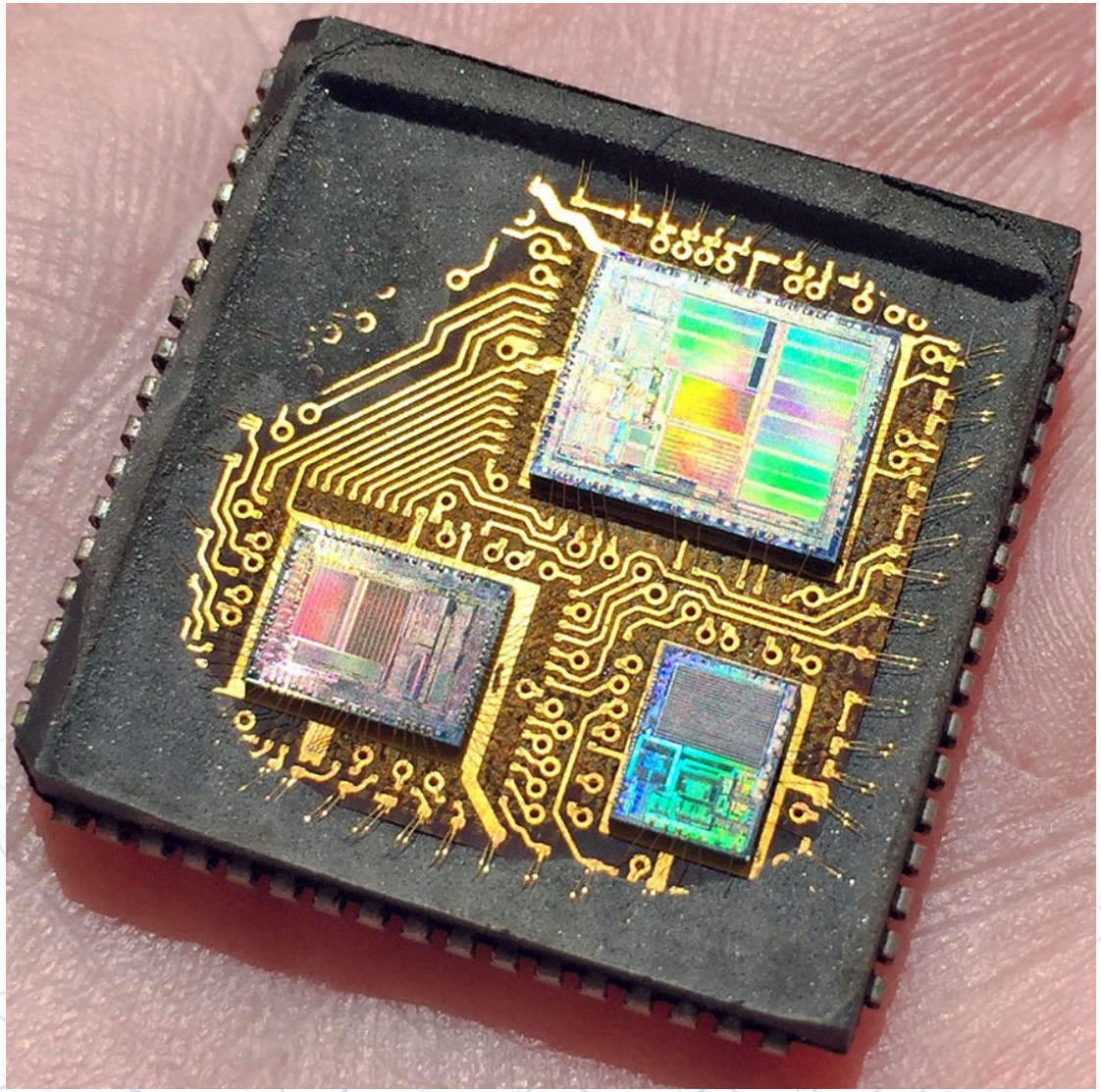
- For smaller form-factor, and higher performance, multiple dies and flip-chips are placed within one substrate
  - Die-stacking was available
  - Locate fingers are placed around each die with minimal wire ponding
  - multiple-layer of substrate using new special films, Ajinomoto Build-up Film





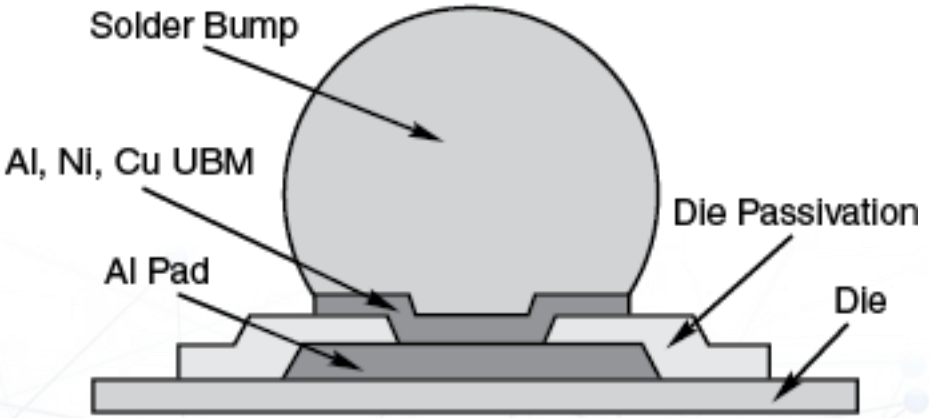
SiP Gallery (From Internet)

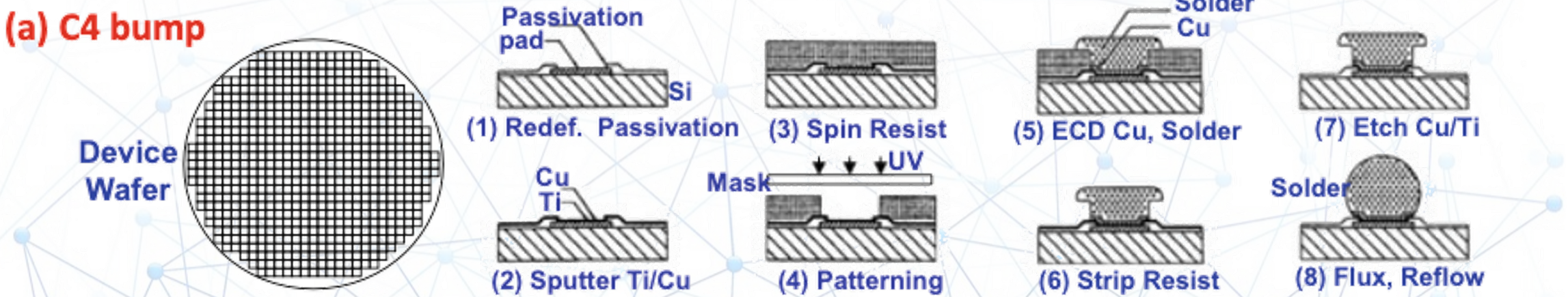




Flip Chip and C4 Bump

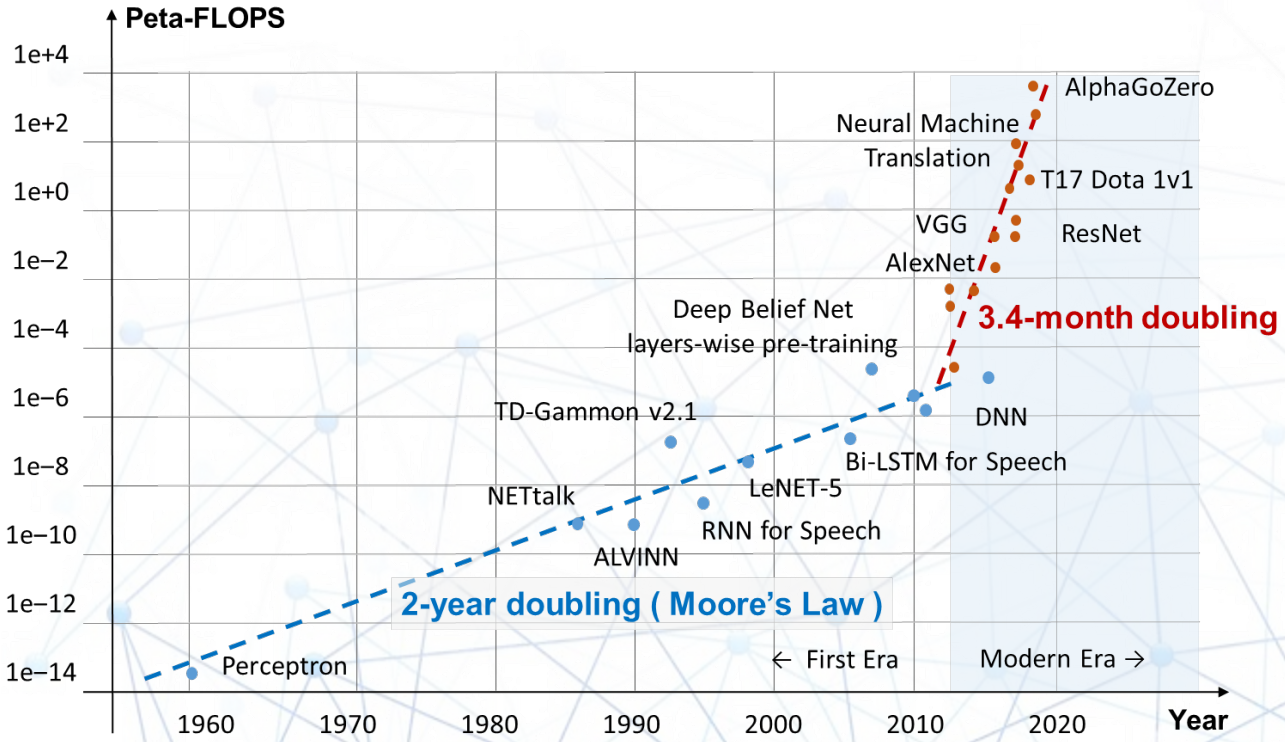
- Today, the controlled collapse chip connection (C4) bumps are the most used interconnection structure.
- C4 bumps uses SnAg and has a pitch of 150 µm, and 90 µm pad opening

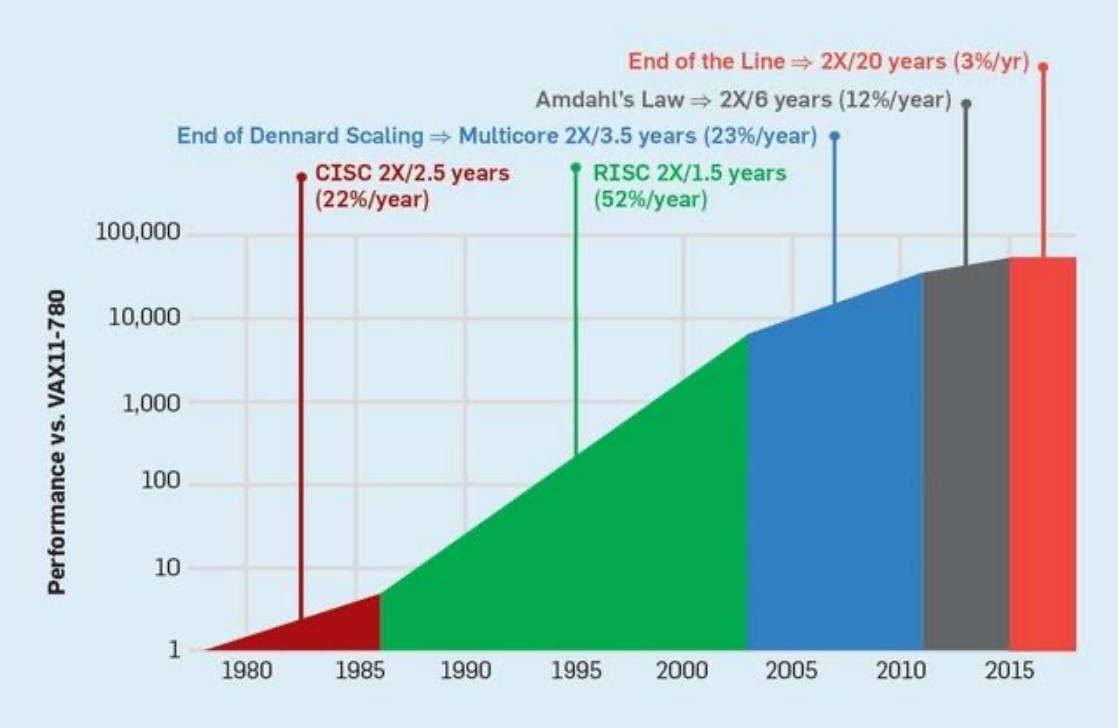




Why We Need More (Than Moore)?

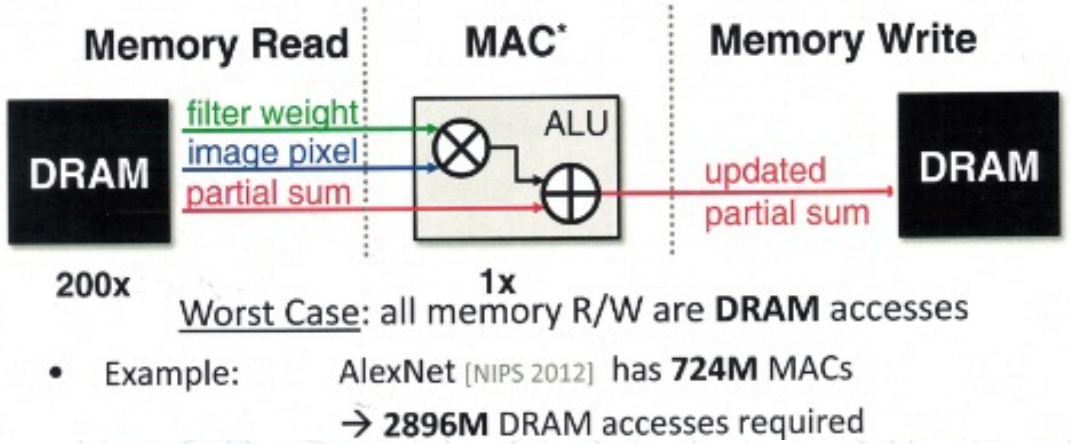
- Deep Learning Algorithm doubles per 3.4 months (10+x every year)
- Moore's Law doubles per 1.5~2 year
- Von-Neumman Architecture (CPU) doubles per 20 years

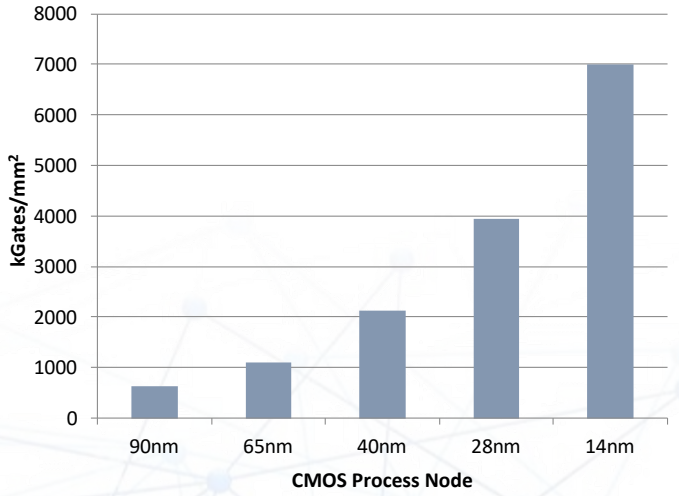




The Interconnect Problem / Memory wall

- High performance computing requires both more logic gates and higher rate processor-memory communication.



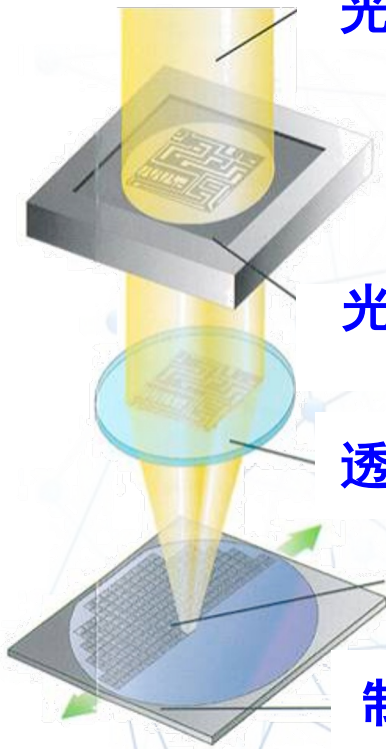


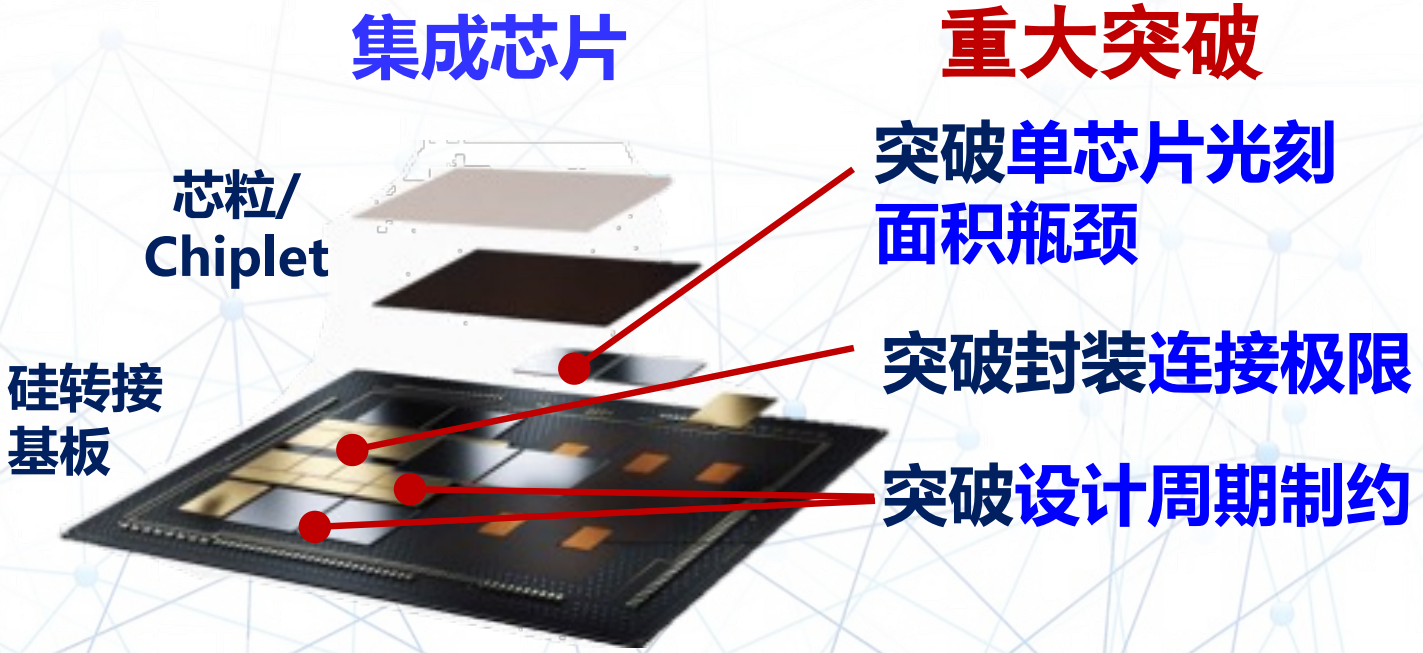
- But memory interface grows more slower than Moore's Law, 16x in 20 years.
  - Logic density increase by 1000x in 20 years.

DDR SDRAM Standard	Release Year	Prefetch Buffer Size	Vdd	Maximum Transfer Rate (MT/s)	Chip Density
DDR1	2000	2n	2.5	200-400	256Mb-1Gb
DDR2	2003	4n	1.8	400-1066	512Mb - 4Gb
DDR3	2007	8n	1.5	1066-2400	1Gb-8Gb
DDR4	2014	8n	1.2	2133-4800	4Gb-32Gb
DDR5	2021 (expected)	16n	1.1	4266-6400	16Gb-32Gb

Monolithic SoC Performance Limit

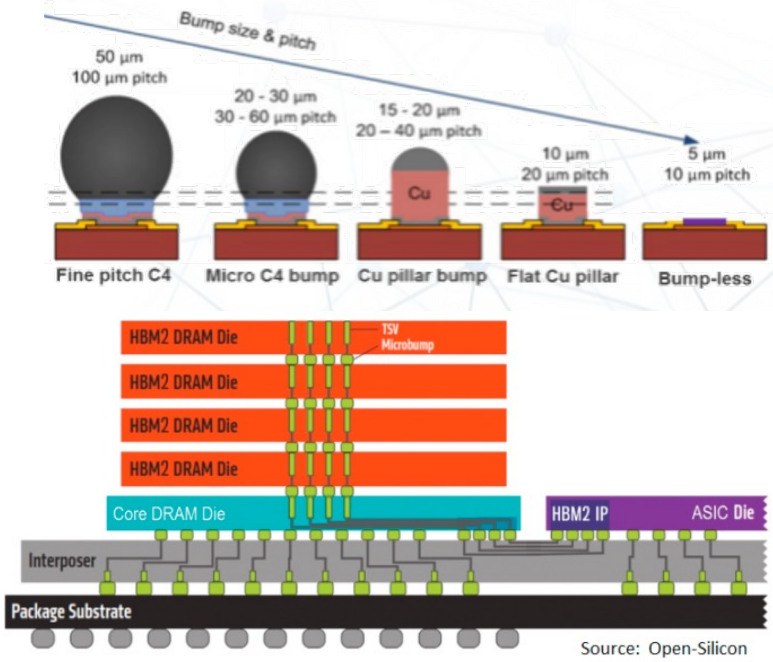
- Monolithic (Single Chip) SoC is limited by the maximum fabrication area due to lithography, known as reticle size (since DUV, it has been 858 mm^2)
- High performance can be obtained either by scaling down or multi-die(chiplet).

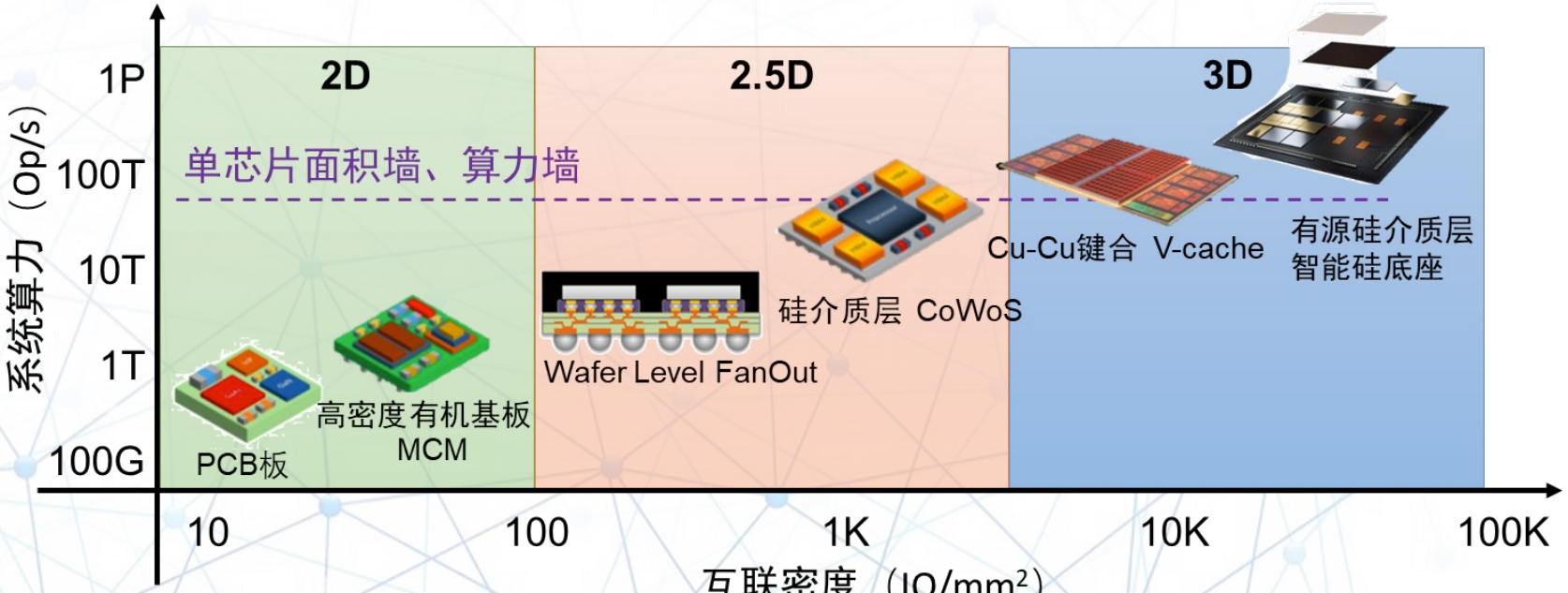




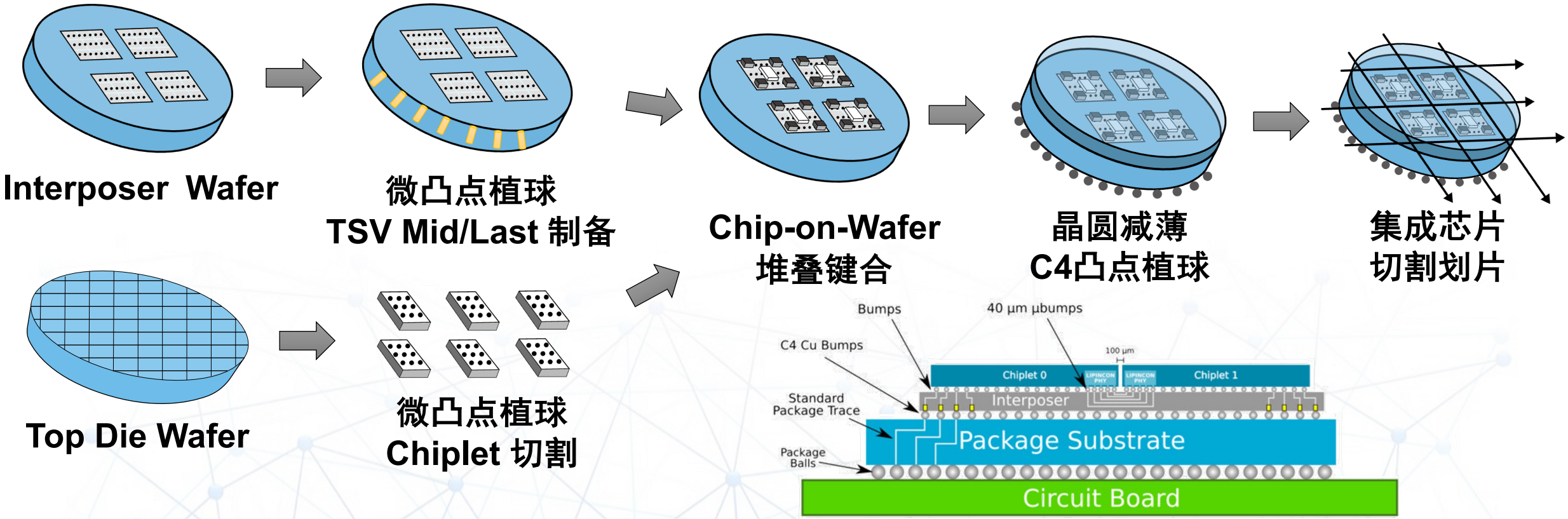
Roadmap of Heterogenous Integration

- Compared with conventional PCB/SiP substrate, advanced packaging introduces semiconductor fabrication technology to implement finer interconnect
- The bump size is reduced to 10um pitch, the line width/space is reduced to sub 1um， therefore the number of interconnect can improve by 10-1000x.



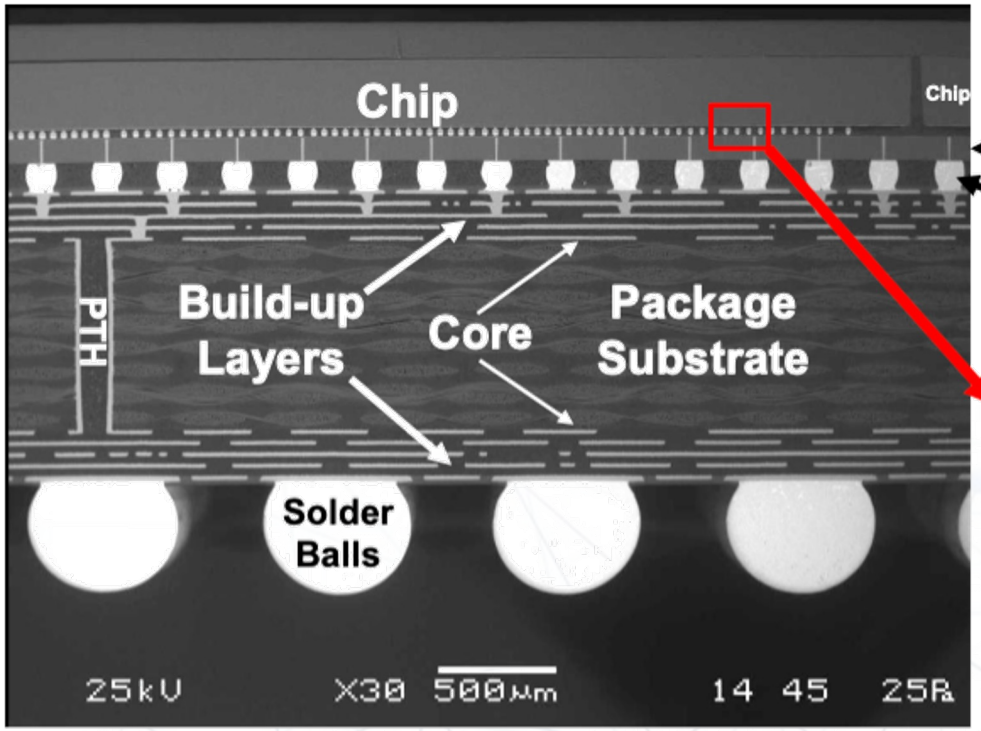


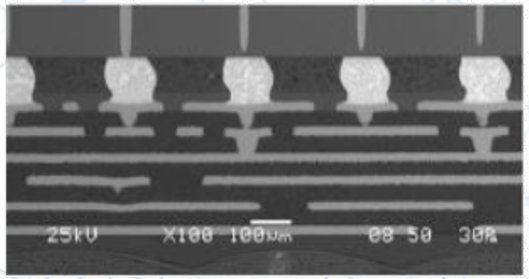
An example of Advanced Packaging （2.5D）



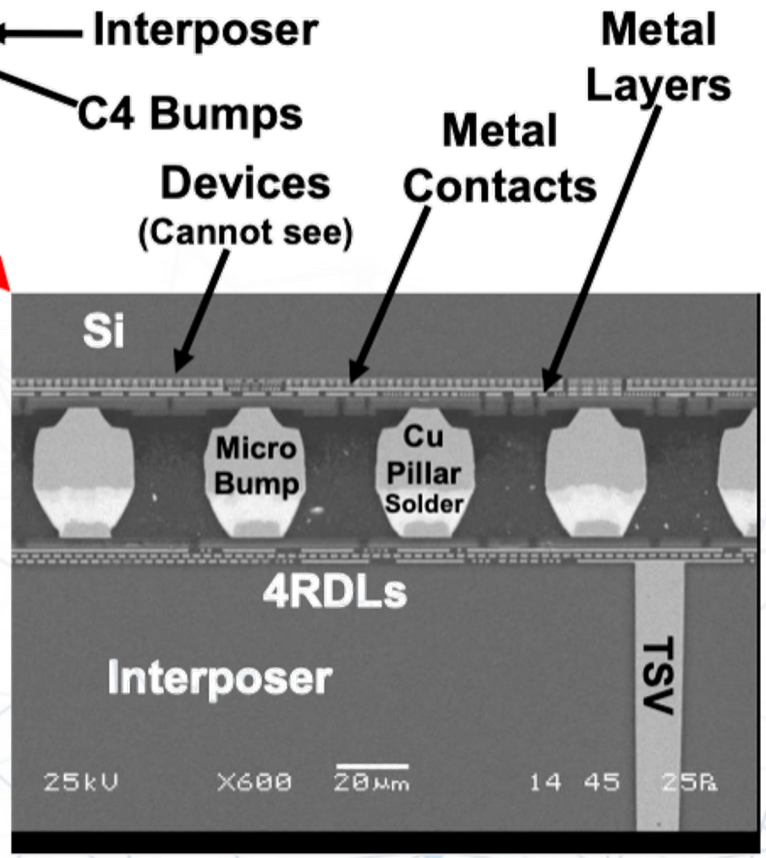
- Silicon interposer (semiconductor wafer) replaces the conventional substrate in advanced packaging.
- Die to wafer bonding / through silicon via (TSV) become new technologies.

Cross section photo of 2.5D Integration





The package substrate is at least (5-2-5)



- RDLs: 0.4µm-pitch line width and spacing
- Each FPGA has >50,000 µbumps on 45µm pitch
- Interposer is supporting >200,000 µbumps

Note the Pitch size
- Micro bump
- C4 bump
- Solder ball

History of Integrated Chips

2010年，台积电蒋尚义提出“先进封装”概念，通过连接两颗芯片，解决带宽问题

MARVELL

2015年，美国Marvell提出“模块化芯片”，后演变为“Chiplet”/芯粒。

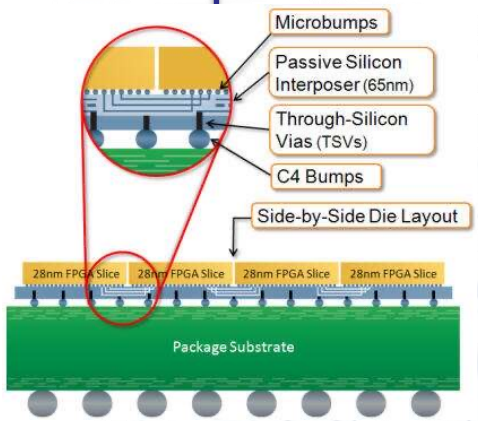
tsmc
台灣積體電路製造股份有限公司
Taiwan Semiconductor Manufacturing Company, Ltd.

2019年，台积电用“System on Integrated Chips”命名“先进封装”。

2021年开始，孙凝晖/刘明/蒋尚义将该理念凝练成“集成芯片”，并于2022年5月在双清论坛上正式发布

2.5D Integrated Chips improves Performance

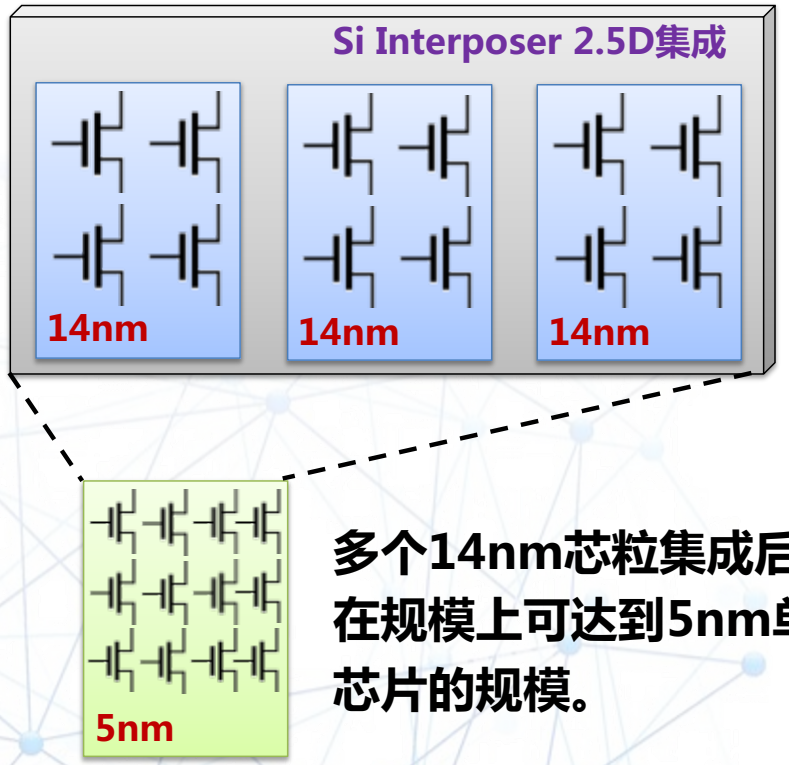
➢2.5D集成技术基于半导体工艺的无源硅Interposer/RDL Interposer/硅桥，大幅缩小互连凸点的尺寸/间距，**增加互连线密度和通信带宽**，并降低延时。



Xilinx V72000T
4颗相同FPGA 芯粒
2.5D集成 2层堆叠
先进封装概念被提出

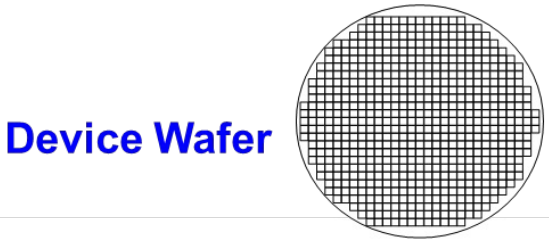
英伟达 GP100
GPU+DRAMx4
2种芯粒共5颗
2.5D集成 2层堆叠

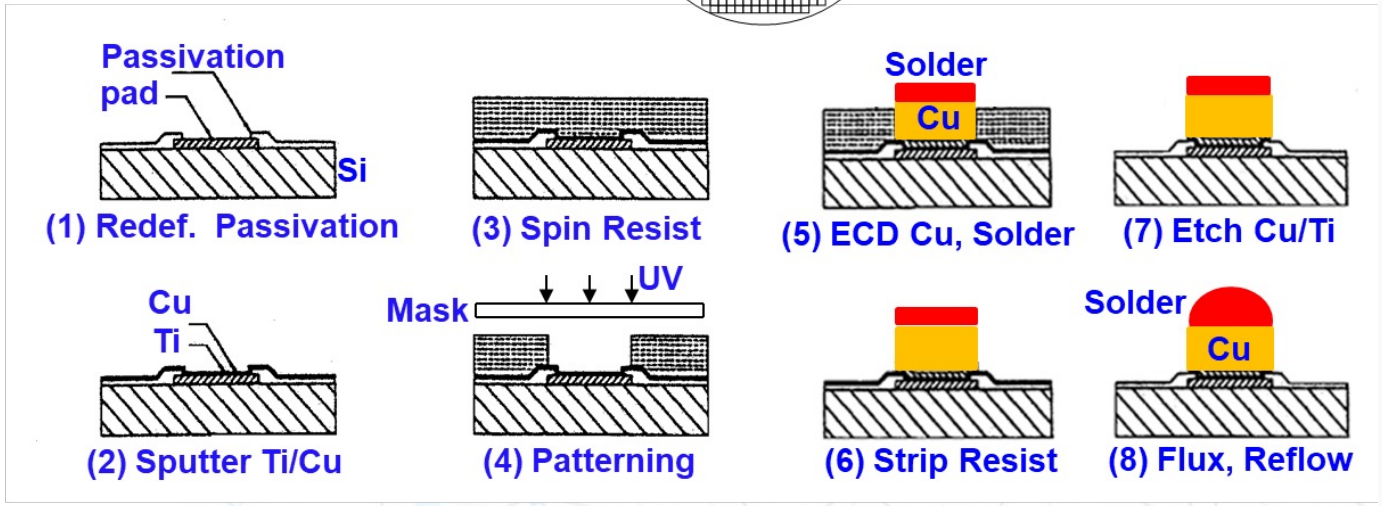
华为 昇腾910
AI+DRAM+IO
3种芯粒共6颗
2.5D集成
2层堆叠

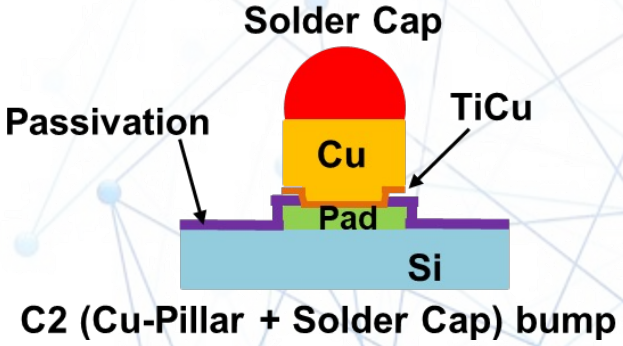


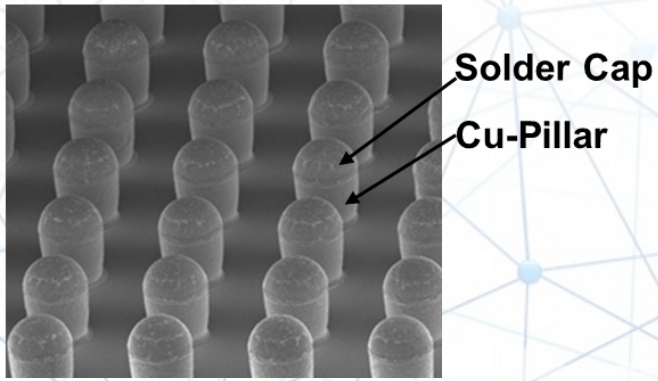
多个14nm芯粒集成后，在规模上可达到5nm单芯片的规模。

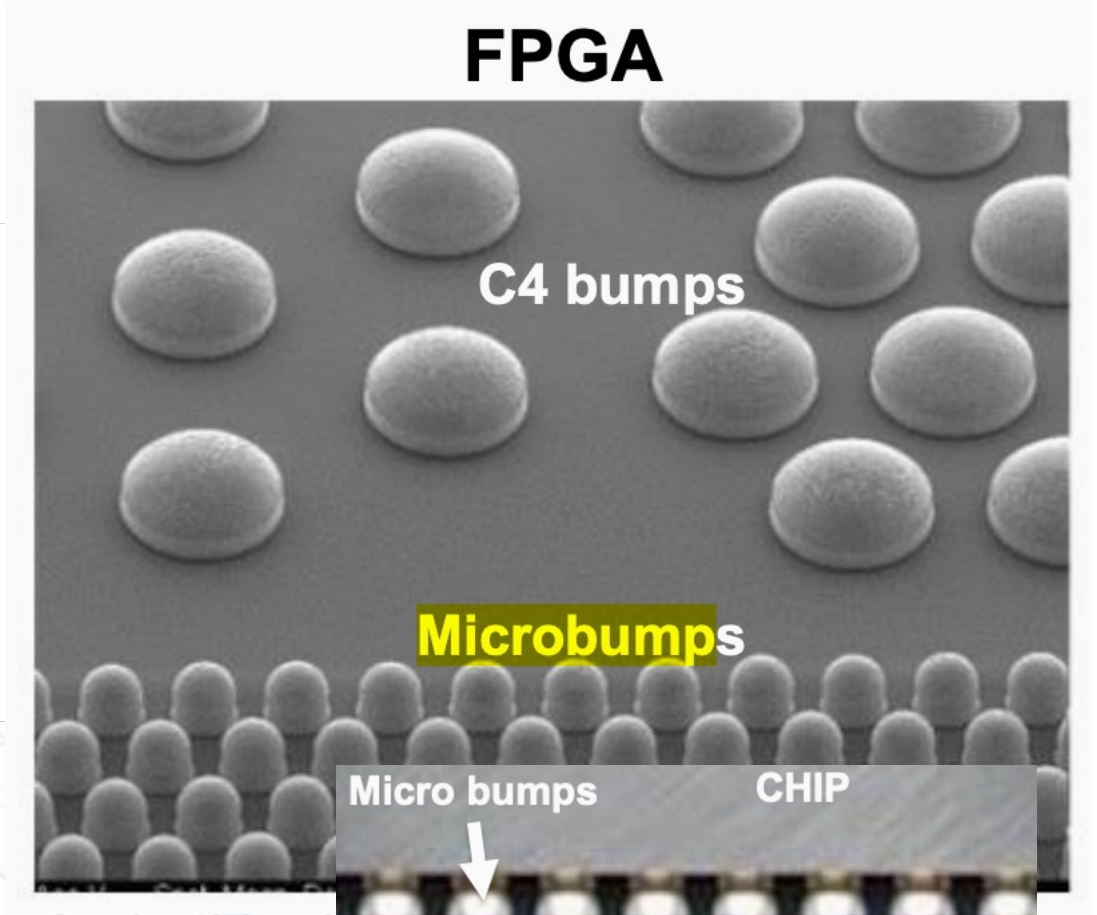
New bump technology (2.5D)







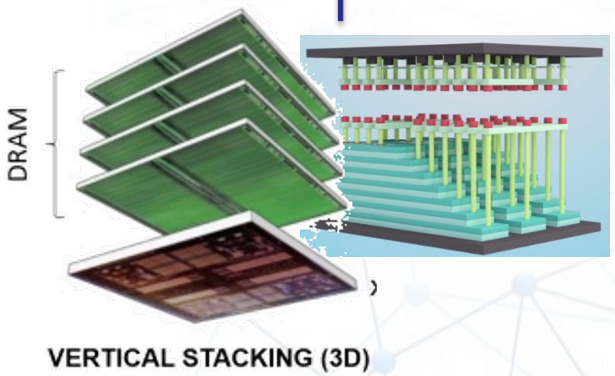




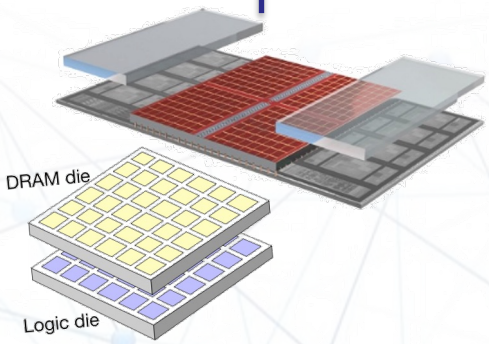
3D Integrated Chips improves Performance

- 3D集成技术通过2个以上芯片的堆叠，实现升维，**提升投影面积上的晶体管密度。**
- 基于上述方法，集成芯片的**能效**提升接近于“摩尔定律”尺寸微缩。

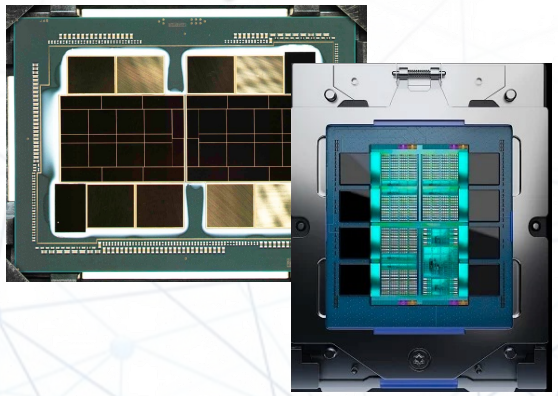
2018年 2021年 2022/23年



三星/海力士 HBM
长江存储 X-Stacking
多层存储3D集成
DRAM/Flash + PHY
高密度存储集成芯片

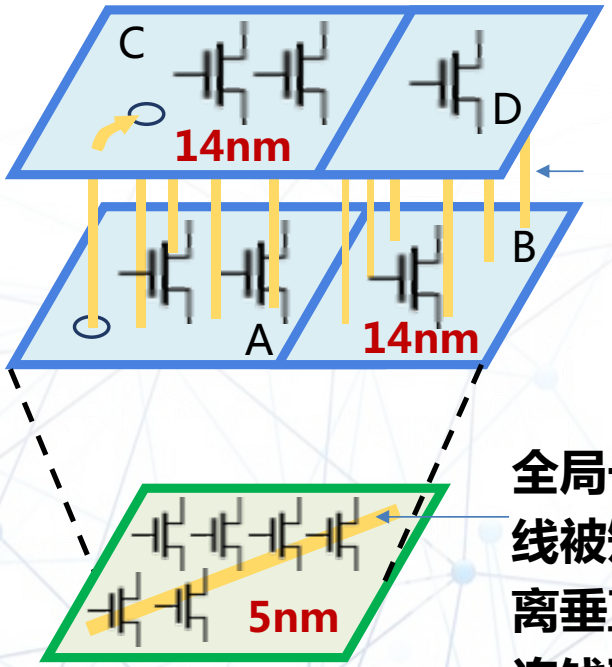


AMD 3D-VCache
平头哥 ML处理器
2层堆叠3D集成
处理器+存储器芯粒
高能效处理器集成芯片



Intel PV AMD MI300
3/4层堆叠3D集成
Base-有源硅Interposer
+ Top - 处理器/存储器芯粒
高性能处理器集成芯片

三维堆叠集成芯片

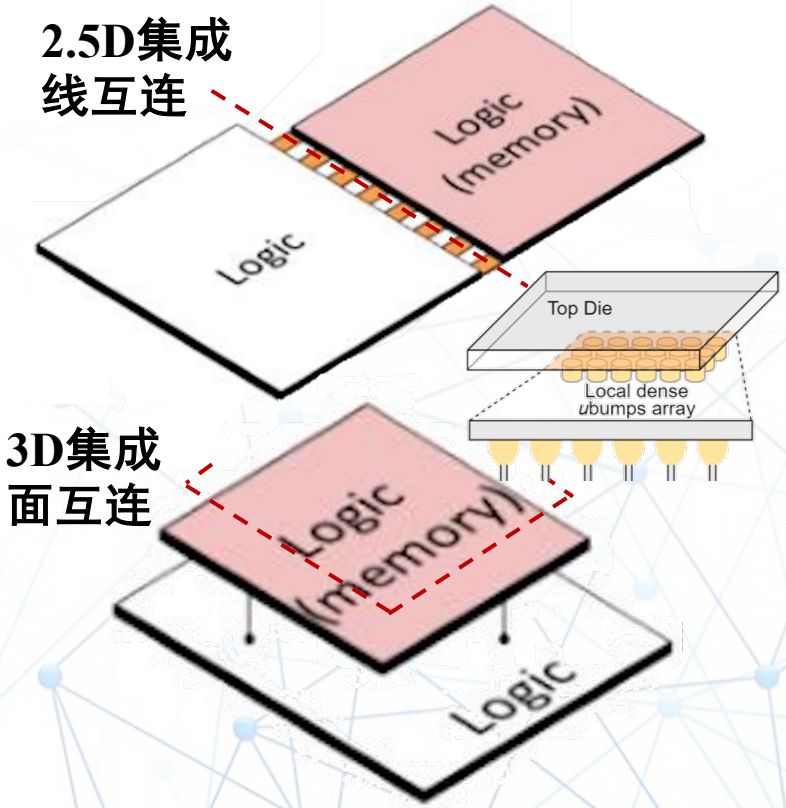


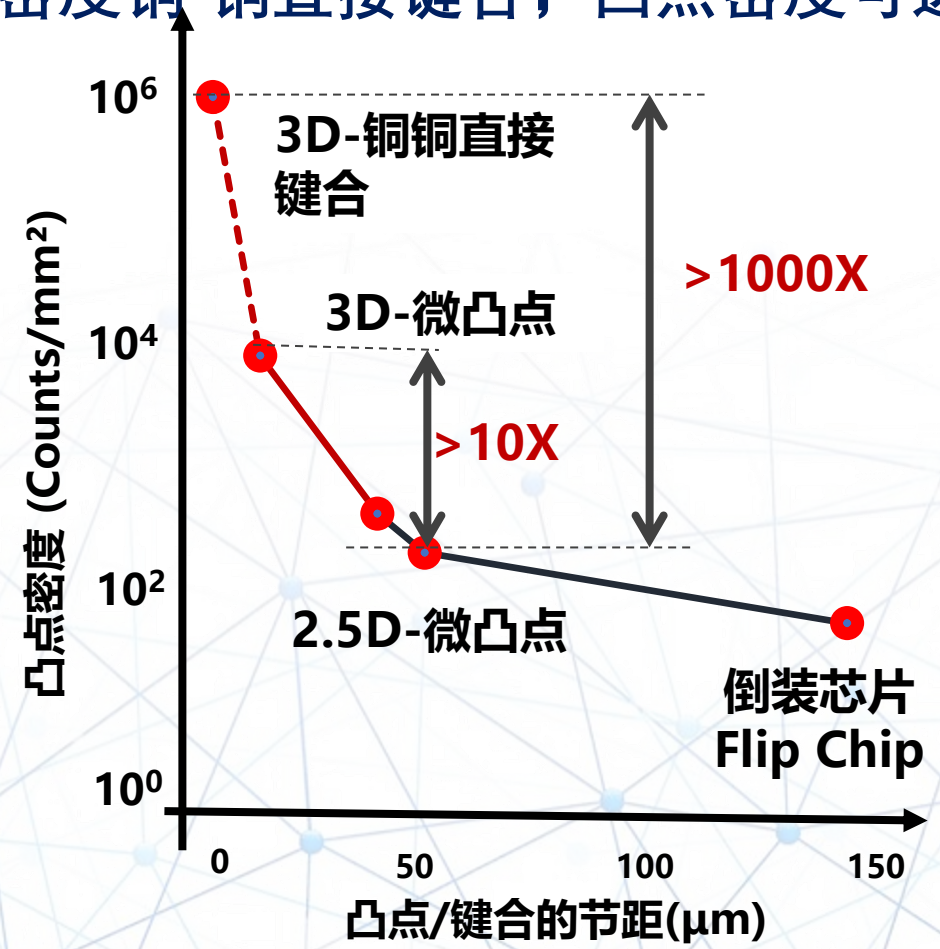
单芯片

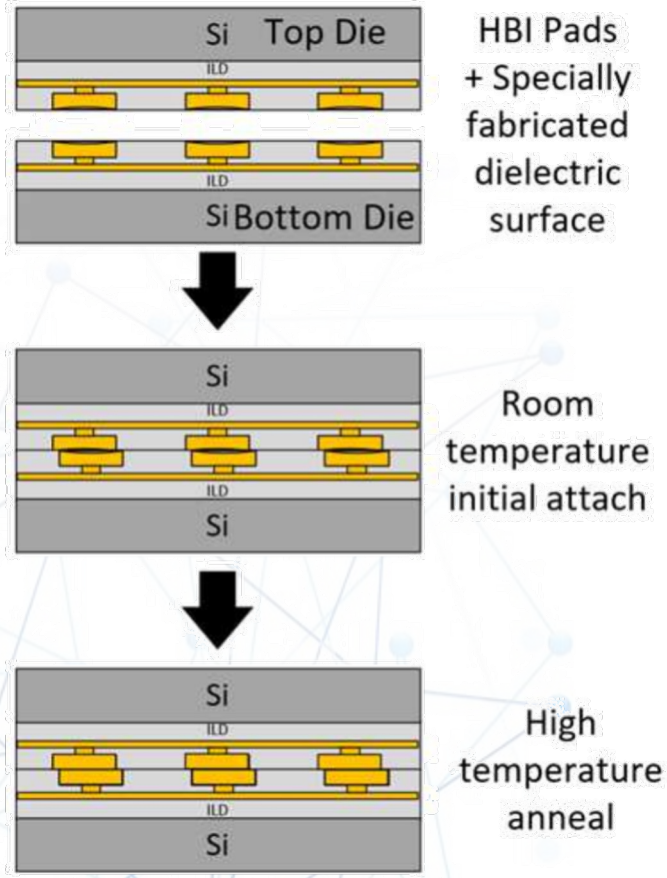
全局长连线被短距离垂直互连钱取代，降低功耗。

3D Integrated Chips improves Performance

- N层三维堆叠集成芯片的逻辑与存储算力密度可提升N倍，（N=2时等效2-3代微缩）
- 三维堆叠的互连界面支持高密度铜-铜直接键合，凸点密度可达10^6个/mm^2。

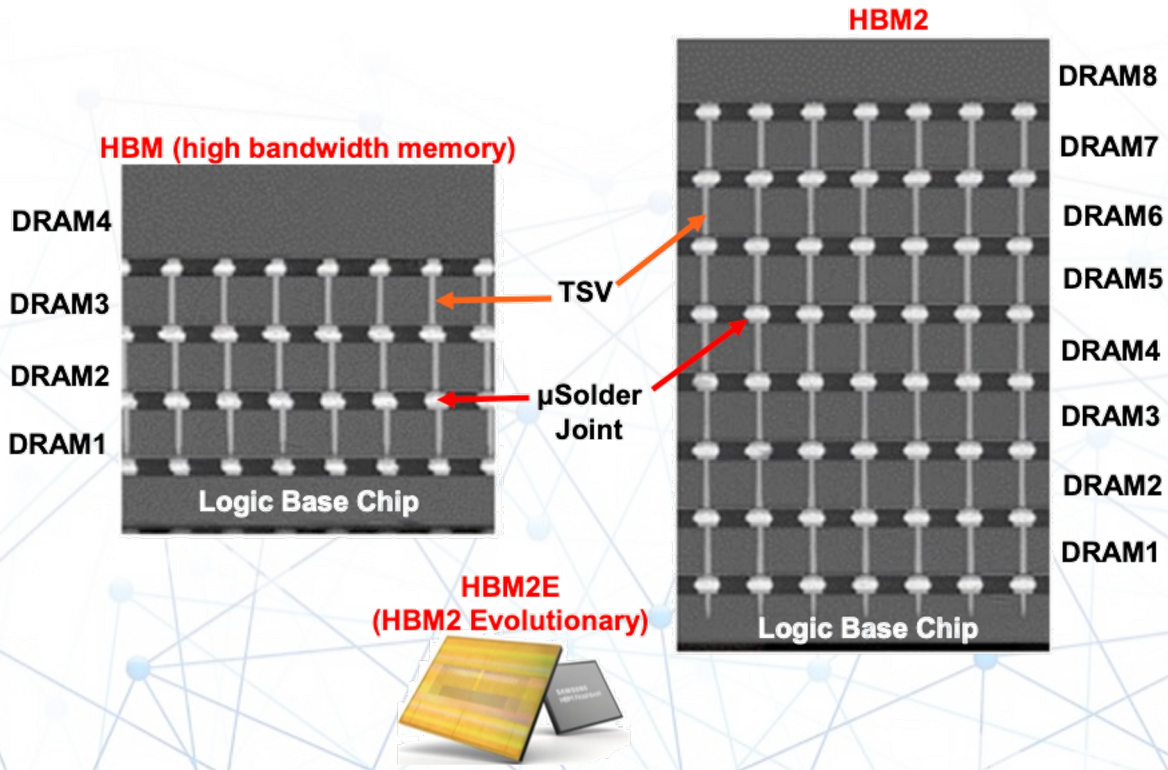


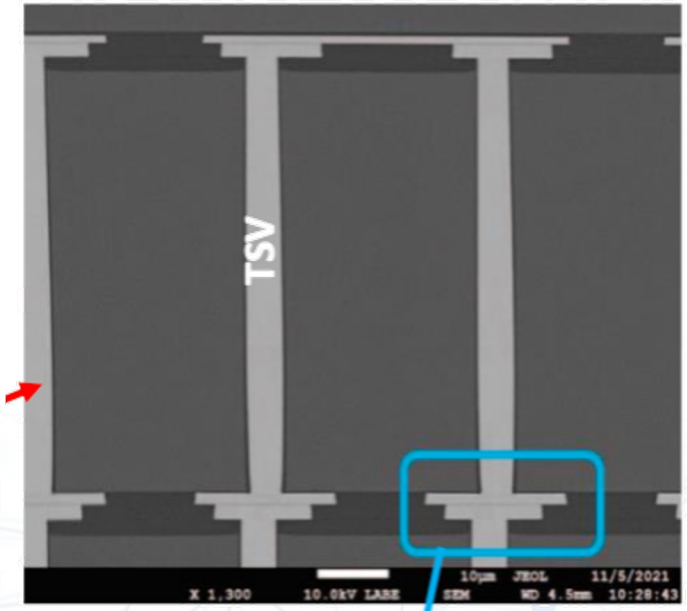




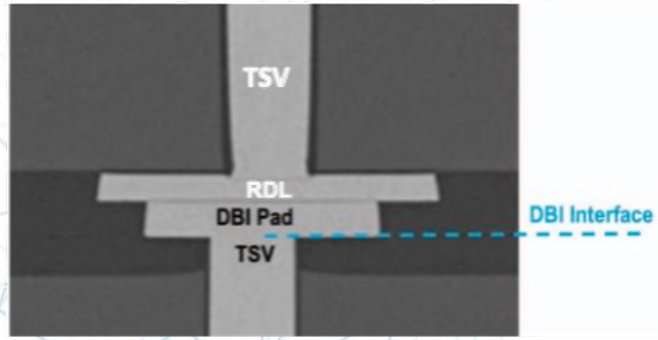
3D Stacking Memory Technology

- High bandwidth memory (DRAM) is a type of multi-die stacking DRAM for 2.5D integrated systems.
- Recent HBM 2e/3 has 8 die stacking.



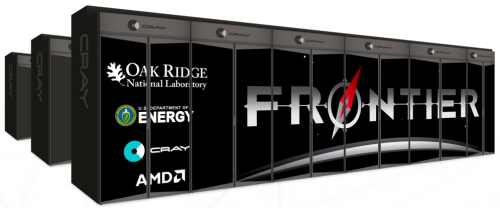
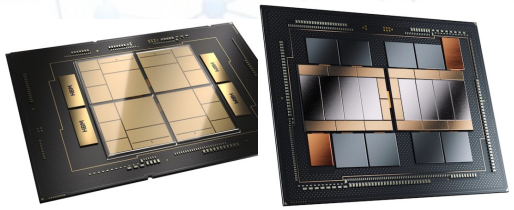
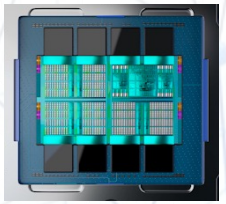
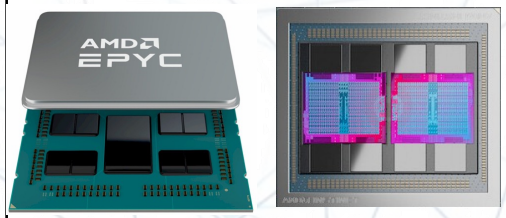
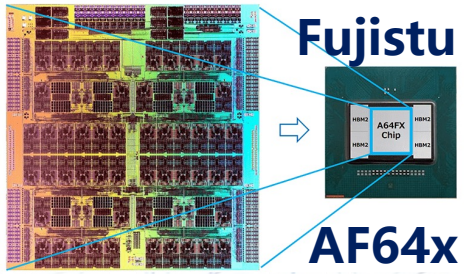


(c)



Integrated Chips is a major trend in HPC chips

➢ Using advanced packaging for high performance computing chip design is a very HOT topic.

排名	2023 新进超算一	2023 新进超算二	2022 Top 500 第一	2022 Top 500 第二
超算中心	 美国 橡树岭 Frontier	 美国 劳伦斯 EL CAPT	 美国 橡树岭 Frontier	 日本 富岳 Fugaku
总算力	2 EFLOPS	2 EFOPS	1.102 EFLOP	0.442 EFLOP
芯片组	 Ponte Viecchio	 MI300/300X	 AMD Zen3+MI250X	 Fujistu AF64x
集成芯片 Chiplet数	GPU+SRAM+HBM +Act Int. (47)	CPU+GPU+HBM +Acttive Int. (21)	CPU：9 智能计算：2+HBMx8	1+HBMx4